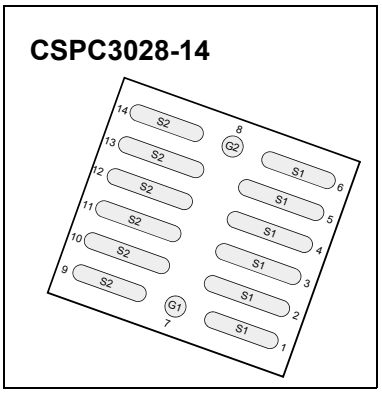
SZCJ Shenzhen Changji Semiconductor Co., LTD.

CSP Enhancement Mode Power MOSFET

CJ12209SP Dual N-Channel MOSFET

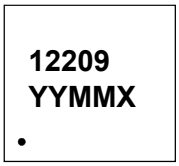
V_{SSS}	$R_{SS(on)}$TYP	I_S
12V	1.2mΩ@4.5V	19.8A
	1.3mΩ@3.8V	
	1.4mΩ@3.1V	
	1.6mΩ@2.5V	



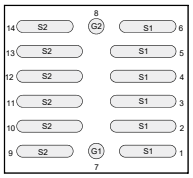
DESCRIPTION

The CJ12209SP uses advanced trench technology to provide excellent $R_{SS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V while retaining a 8V $V_{GS(MAX)}$ rating. It is ESD protected. This device is suitable for use as a unidirectional or bi-directional load switch, facilitated by its common-drain configuration.

Marking and pin assignment





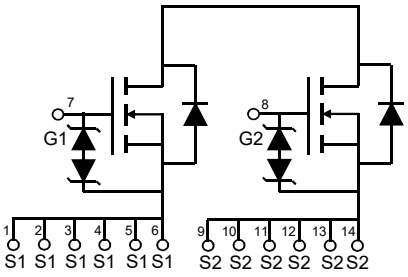


Marking:

1. 12209: Product Code
2. YYMMX: Date Code
3. Solid dot: Pin 1

1,2,3,4,5,6 Source1
9,10,11,12,13,14 Source2
7 Gate1
8 Gate2

Equivalent Circuit



ABSOLUTE MAXIMUM RATINGS (T_a=25℃ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Source to Source Voltage	V_{SSS}	12	V
Gate-Source Voltage	V_{GSS}	±8	V
Source Current(DC)	I_S ①	19.8	A
Source Current (Pulsed)	I_{SP} ①②	198	A
Total Power Dissipation	P_T ①	3.1	W
Channel Temperature	T_{ch}	150	℃
Storage Temperature Range	T_{STG}	-55 To 150	℃

MOSFET ELECTRICAL CHARACTERISTICS

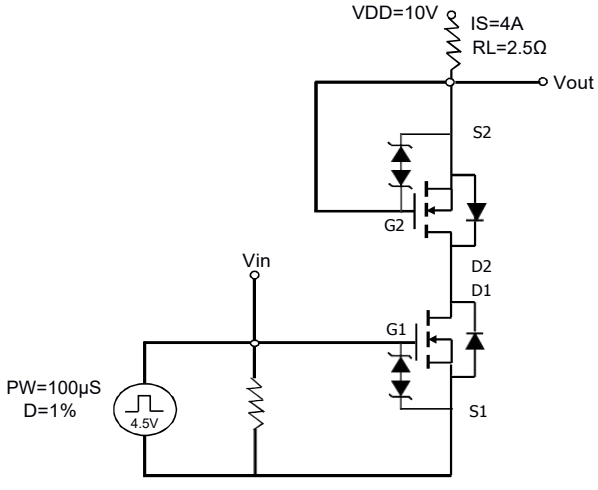
T_a=25 ℃ unless otherwise specified

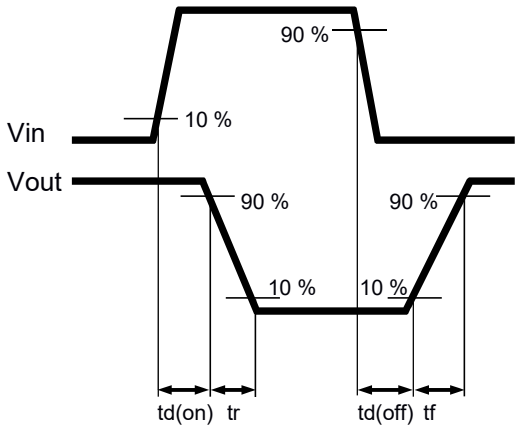
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static Parameters						
Source to Source Breakdown Voltage	BV_{SSS}	I_S=1mA ,V_{GS}=0V	12			V
Zero-Gate Voltage Source Current	I_{SSS}	V_{SS}=10V,V_{GS}=0V			1.0	μA
Gate to Source Leakage Current	I_{GSS}	V_{SS}=0V, V_{GS}= ±8V			±10	μA
Gate to Source Threshold Voltage ③	V_{TH}	V_{S2S1}=6V, I_{S1}=2.3mA	0.35	0.77	1.4	V
		V_{S1S2}=6V, I_{S2}=2.3mA				
Source to Source On-state Resistance	$R_{SS(on)}$	V_{GS}=4.5V,I_S=3A	0.8	1.2	1.56	mΩ
		V_{GS}=3.8V,I_S=3A	0.9	1.3	1.69	mΩ
		V_{GS}=3.1V,I_S=3A	1.0	1.4	1.82	mΩ
		V_{GS}=2.5V,I_S=3A	1.1	1.6	3.20	mΩ
Input Capacitance	Ciss	V_{SS}=10V, V_{GS}=0V,f=1kHZ		6315		pF
Output Capacitance	Coss			1393		pF
Reverse Transfer Capacitance	Crss			1106		pF
Turn-on Delay Time	$t_{d(on)}$ ③	V_{DD}=10V,I_S=4A, V_{GS}=4.5V		1.2		μS
Turn-on Rise Time	t_r ③			5.7		μS
Turn-off Delay Time	$t_{d(off)}$ ③			11		μS
Turn-off Fall Time	t_f ③			15.4		μS
Total Gate Charge	Q_g ③	V_{SS}=10V,I_S=10A,V_{GS}=4.5V		75		nC
Gate1-source1 charge	Q_{g1s1} ③			15		nC
Gate1-source2 charge	Q_{g1s2} ③			36		nC
Diode Forward Voltage	$V_{F(S-S)}$	V_{G1S1}=0V,V_{G2S2}=4.5V,I_S=3A			1.0	V
		V_{G1S1}=4.5V,V_{G2S2}=0V,I_S=3A				

Notes: 1.Mounted on FR4 board (25.4mm×25.4mm×t1.0mm) using the minimum recommended pad size (36um Copper).

2.t = 10 ms , Duty Cycle = 1 %.

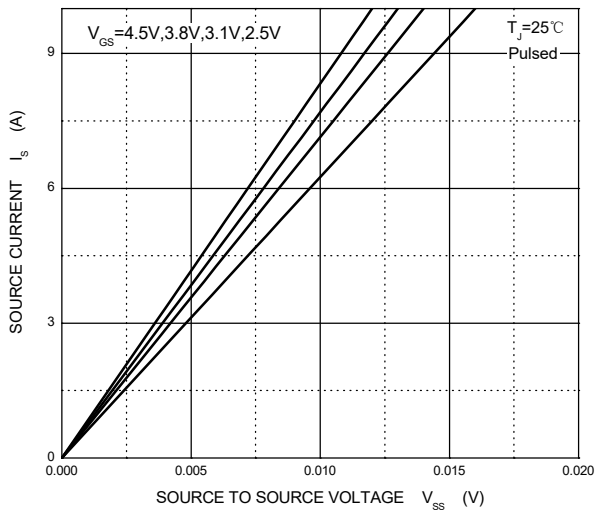
3.When FET1 is measured,G2 and S2 are short-circuited.



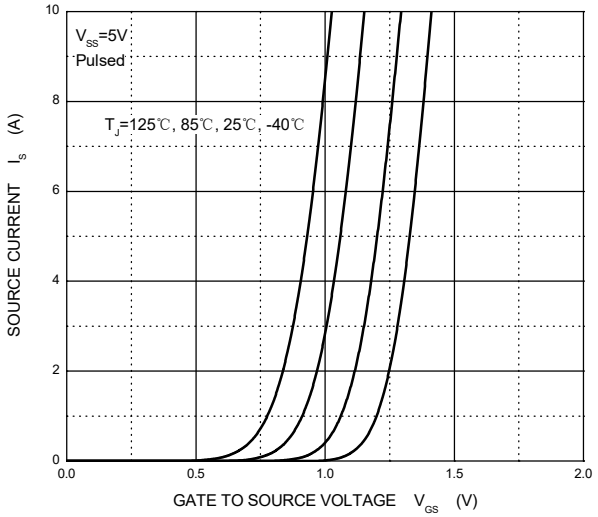


Typical Characteristics

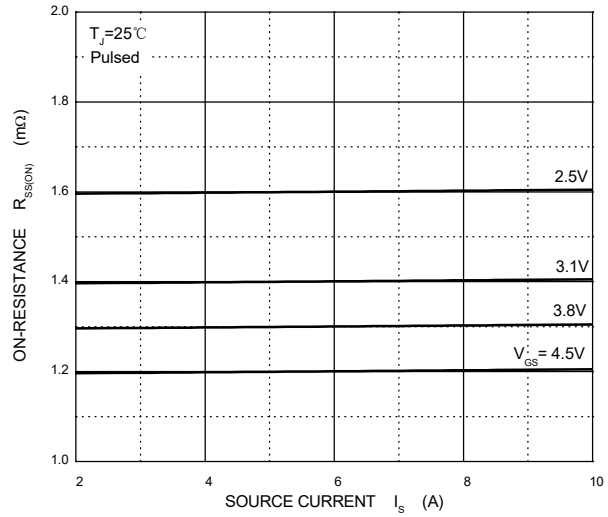
IS -- VSS



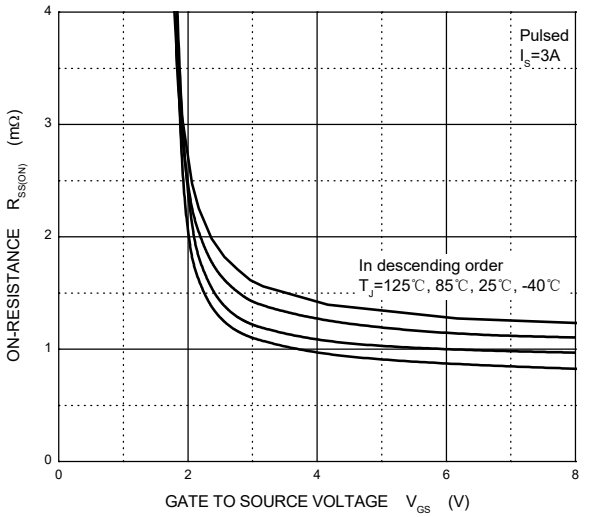
IS-VGS



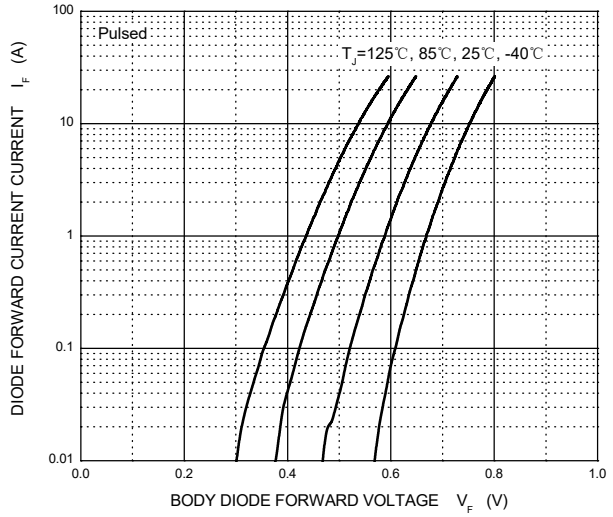
$R_{SS(ON)}$ —— I_S



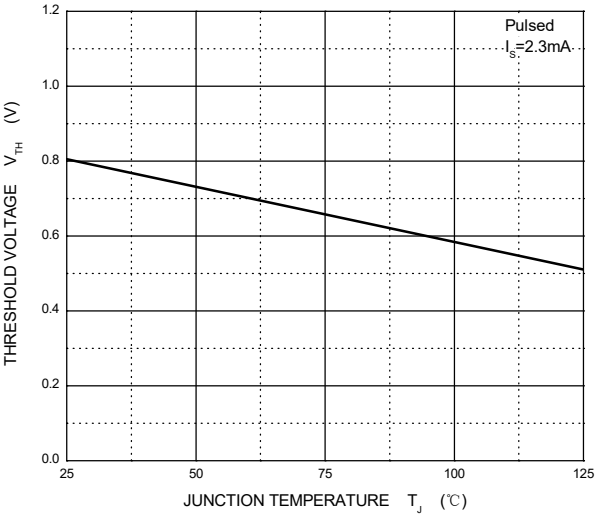
$R_{SS(ON)}$—— V_{GS}



I_F —— V_F

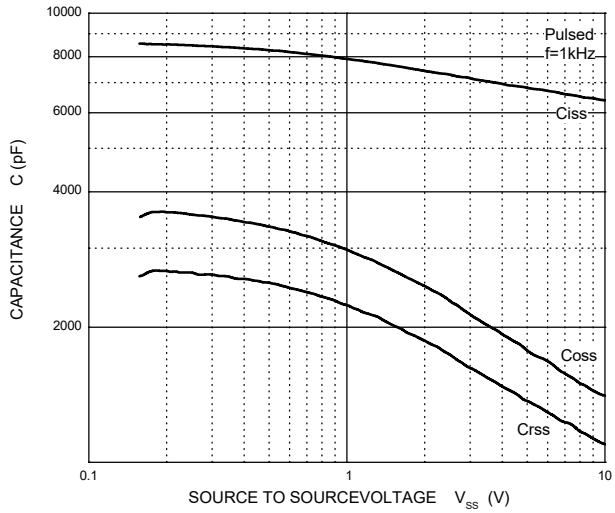


Threshold Voltage

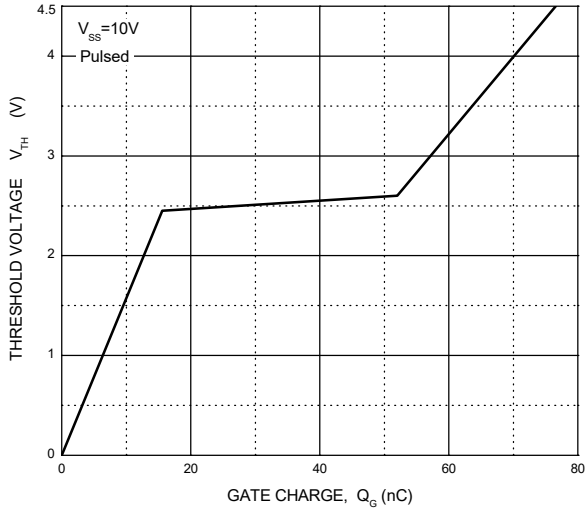


Typical Characteristics

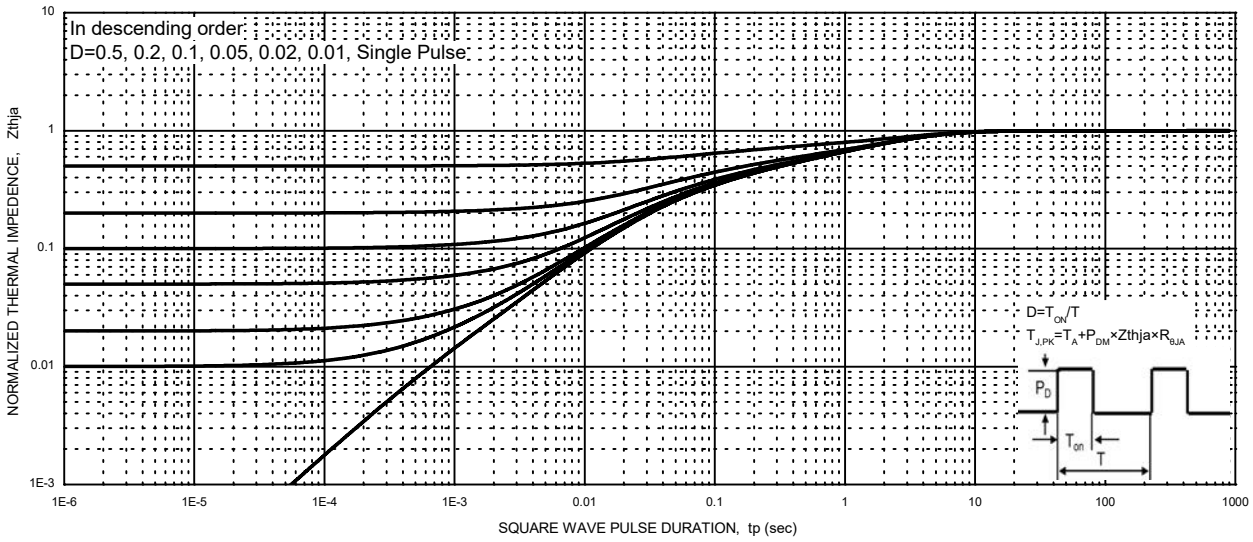
Capacitances



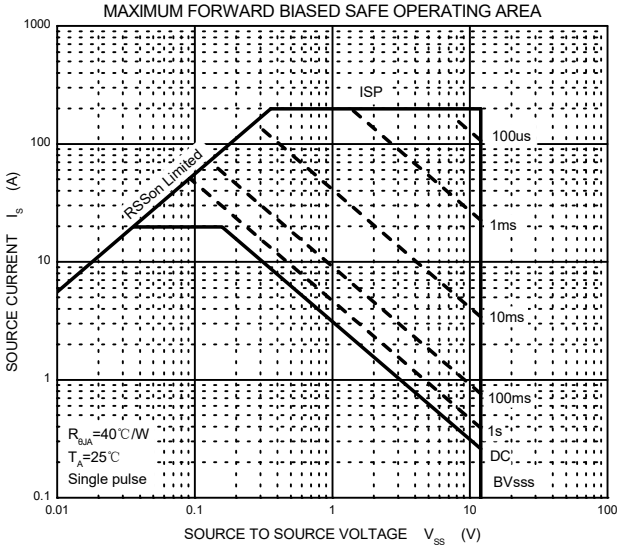
Gate Charge



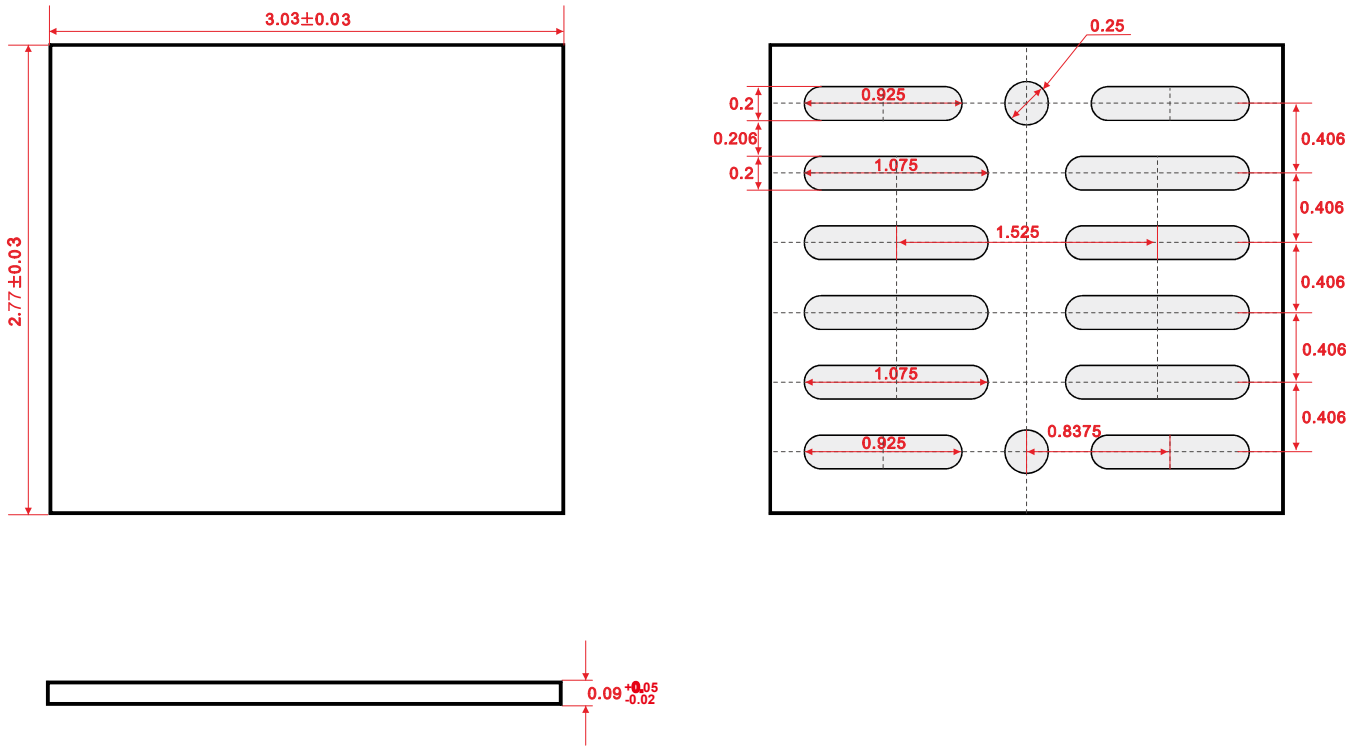
NORMALIZED TRAISIENT THERMAL IMPENDANCE



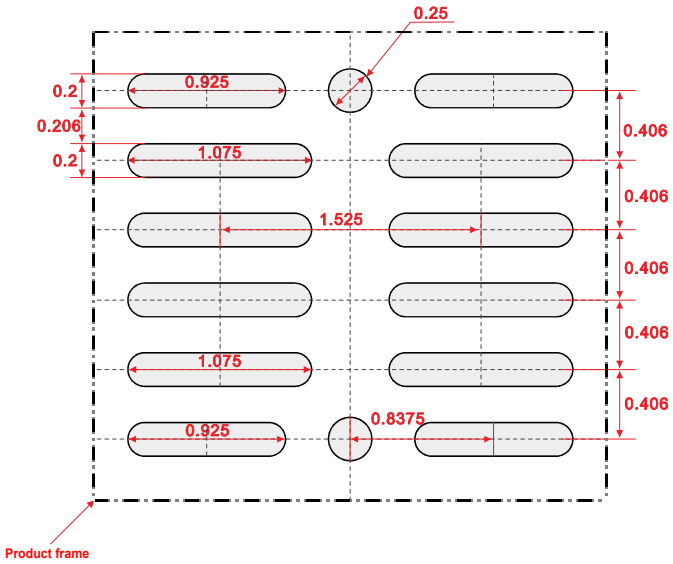
MAXIMUM FORWARD BIASED SAFE OPERATING AREA



CSPC3028-14 Package Outline Dimensions(Unit:mm)



CSPC3028-14 Suggested Pad Layout (Unit:mm)

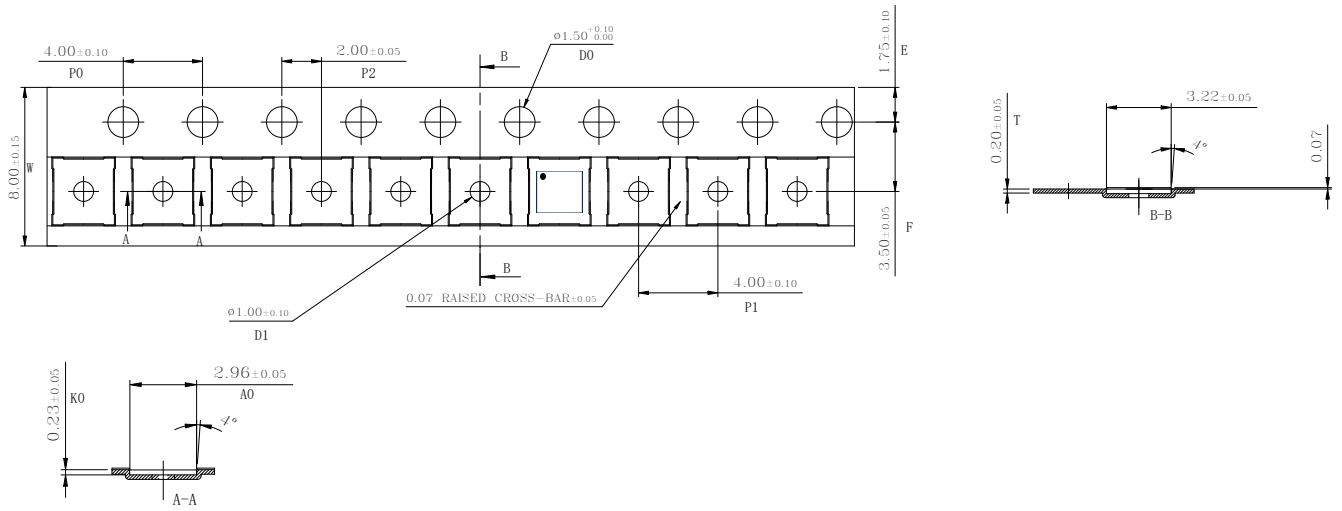


Note:
1.Controlling dimension:in millimeters.
2.General tolerance:± 0.050mm.
3.The pad layout is for reference purposes only.

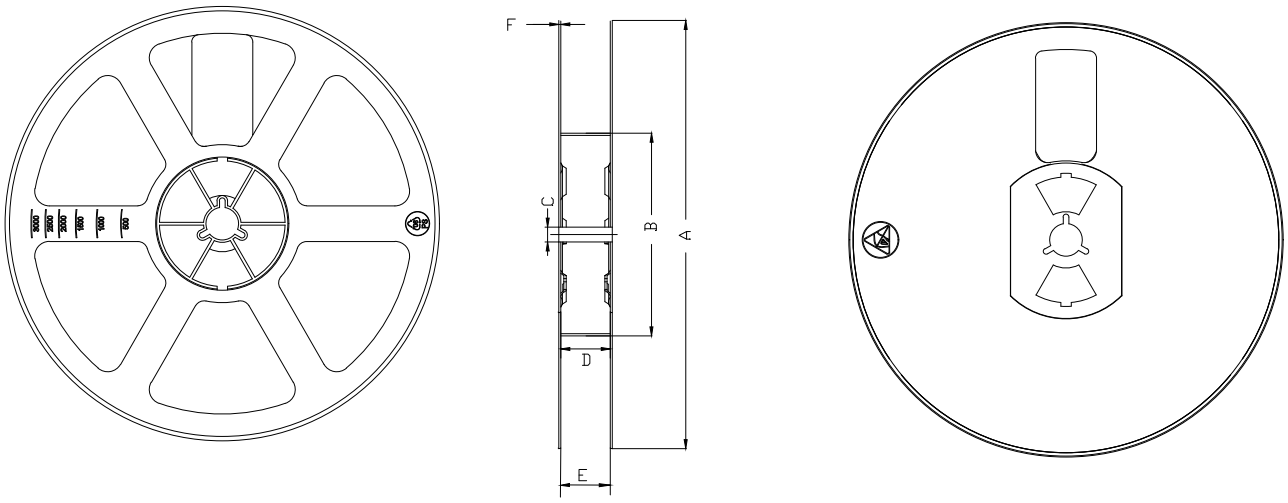
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Tape and Reel



产品尺寸规格 (UNIT:mm)						
规格	A0	B0	K0	P0	P1	P2
尺寸	2.96±0.1	3.22±0.05	0.23±0.05	4.0±0.1	4.0±0.1	2.0±0.05
规格	T	E	F	D0	D1	W
尺寸	0.2±0.05	1.75±0.1	3.5±0.05	$1.5^{+0.1}_{0.0}$	1.00±0.1	8.0±0.15



SIZE	8MM
A	178±2.0
B	55±1.0
C	$13.0^{+0.35}_{-0.15}$
D	$8.4^{+2.5}_{-0.4}$
E	$8.65^{+4.7}_{-0.65}$
F	1.5±0.5

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