Standalone Linear Li-Ion Battery Charger with Thermal Regulation

CJ4054 Series

■ INTRODUCTION:

The CJ4054 is a complete constant-current/ constant –voltage linear charger for single cell lithium-ion batteries. Its SOT package and low external component count make the CJ4054 ideally suited for space limited portable applications.

Furthermore, the CJ4054 is specifically designed to work within USB power specifications.

No external sense resistor is needed, and no blocking diode is required due to the internal MOSFET architecture. Thermal feedback regulates the charge current to limit the die temperature during high power operation or high ambient temperature. The charge voltage is fixed at V_{FLOAT}, and the charge current can be programmed externally with a single resistor connectd between PROG pin and GND. The CJ4054 automatically terminates the charge cycle when the charge current drops to 1/10th the programmed value after the final float voltage is reached. When the input supply (wall adapter or USB supply) is removed, the CJ4054 automatically enters a low current state, dropping the battery drain current to less than 2μA. The CJ4054 can be put into shutdown mode, reducing the supply current to 25μA. Other features include charge current monitor, undervoltage lockout, automatic recharge and a status pin to indicate charge termination.

■ FEATURES:

- Ideal for Low-Dropout Designs for Single-Cell Li-Ion or Li-Pol Batteries Charge Directly from USB Port or AC Adapter in Space Limited Portable Applications
- Integrated P-ch Power MOSFET and Current Sensor for Up to 800mA Charge Applications
- Reverse Leakage Protection Prevents Battery Drainage
- Pre-charge Conditioning for Reviving Deeply Discharged Cells and Minimizing Heat Dissipation During Initial Stage of Charge
- 2.9V Trickle Charge Threshold
- Constant-Current/Constant-Voltage operation with Thermal Regulation Maximizes Charge Rate Without Risk of Overheating
- Integrated Current and Voltage Regulation
  ±10% Current Regulation Accuracy
  ±1% Voltage Regulation Accuracy
- Charge Current Monitor Output for Gas Gauging
- C/10 Charge Termination
- Automatic Recharge
- Status Output for LEDs or System Interface Indicates Charge and Fault Conditions
- Automatic Sleep Mode for Low-Power Consumption
- 25μA Supply Current in Shutdown
- Battery Short-Circuit Protection
- Soft-Start Limits Inrush Current
- Charge Voltage Options: 4.20V and 4.35V

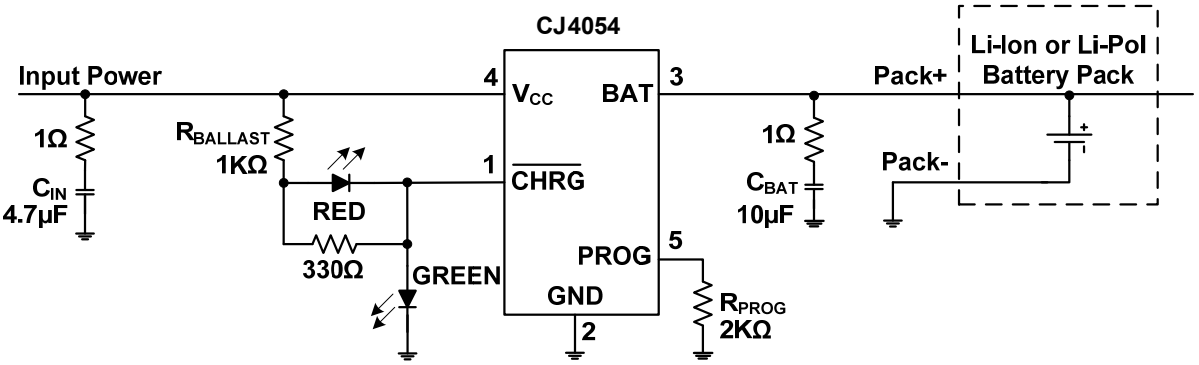
● APPLICATIONS:

- Cellular Telephones, PDAs, MP3 Players
- Digital Still Cameras
- Charging Docks and Cradles
- Bluetooth Applications

■ ORDER INFORMATION(1)

Device No.	Battery Float Voltage	Package	Packaging
CJ4054A420M	4.20V	SOT-23-5L	3000 parts per reel
CJ4054A435M	4.35V	SOT-23-5L	3000 parts per reel
CJ4054A420P	4.20V	SOT-89-5L	1000 parts per reel

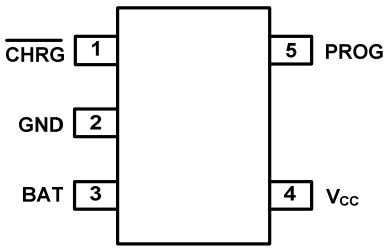
■ TYPICAL APPLICATION CIRCUIT



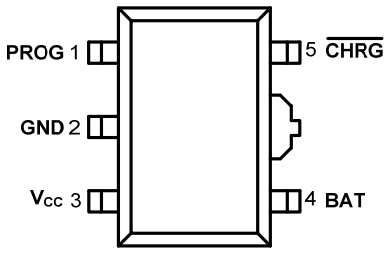
Typical Application for Charging Between 100mA and 500mA

Figure 1. Standard Application Circuit

■ PIN CONFIGURATION



SOT-23-5L (Top View)



SOT-89-5L (Top View)

Electrical Characteristics

Table 1. Pin Description

PIN		NAME	TYPE(1)	DESCRIPTION AND REQUIRED COMPONENTS
No.				
SOT-23-5L	SOT-89-5L			
1	5	$\overline{\text{CHRG}}$	O	**Open Drain Charge Status Output**. When the battery is being charged, the CHRG pin is pulled low by an internal N-channel MOSFET switch. When the CJ4054 detects an undervoltage lockout condition, $\overline{\text{CHRG}}$ pin is forced high impedance.
2	2	GND	I	**Ground Terminal**.
3	4	BAT	I/O	**Charger Power Stage Current Output and Battery Voltage Sense Input**. BAT pin provides charge current to the battery and regulates the final float voltage. An internal precision resistor divider from this pin sets the float voltage which is disconnected in shutdown mode. Connect the positive terminal of the battery to BAT pin. Bypass BAT to GND with 10μF to 47μF capacitor. BAT pin draws less than 2μA current in shutdown mode (R_{PROG} not connected) or sleep mode .
4	3	V_{CC}	I	**Charger Positive Input Supply Voltage and Internal Supply**. V_{CC} is the power supply to the internal circuit. V_{CC} can range from 4.5V to 6.5V and should be bypassed with at least a 4.7μF capacitor. When V_{CC} drops to within 80mV of the BAT pin voltage, the CJ4054 enters low power sleep mode, dropping BAT pin's current to less than 2μA.
5	1	PROG	O	**Charge Current Program, Charge Current Monitor and Shutdown Pin**. The charge current is programed by connecting a 1% accuracy metal film resistor R_{PROG} from this pin to GND. When charging in pre-conditioning mode, the PROG pin voltage is regulated to 0.1V. When charging in constant-current mode, the PROG pin voltage is regulated to 1V.In all modes during charging, the voltage on PROG pin can be used to measure the charge current as the following formula: $I_{BAT}=1000V_{PROG}/R_{PROG}$ The PROG pin can also be used to shut down the charger. Disconnecting the program resistor from ground allows a 0.15μA current to pull the PROG pin high. When it reaches the 1.21V shutdown threshold voltage, the charger enters shutdown mode, charging stops and the input supply current drops to 25μA. This pin is also clamped to approximately 2.4V. Driving this pin to voltages beyond the clamp voltage will draw currents as high as 1.5mA. Reconnecting R_{PROG} to ground will return the charger to normal operation.
-	-	NC	-	**No Connect.**

(1) I = Input; O = Output; P = Power

■ ABSOLUTE MAXIMUM RATINGS(1) (unless otherwise specified , T_A=25°C)

PARAMETER		SYMBOL	RATINGS	UNITS
Input Supply Voltage(2)		V_{CC}	-0.3~10	V
PROG Pin Voltage(2)			-0.3~V_{CC}+0.3	
BAT Pin Voltage(2)			-0.3~8	
$\overline{CHRG}$ Pin Voltage(2)			-0.3~10	
BAT Short-Circuit Duration		-	Continuous	-
BAT Pin Output Current (Continuous)		I_{BAT}	800	mA
Output sink current		$I_{\overline{CHRG}}$	10	mA
Power dissipation	SOT-23-5L	P_D	400	mW
	SOT-89-5L	P_D	800	mW
Operating Ambient Temperature Range(3)		T_A	-40~85	°C
Junction Temperature		T_J	-40~125	°C
Storage Temperature		T_{stg}	-65~125	°C
Lead Temperature (Soldering, 10s)		T_{solder}	260	°C
ESD rating(4)		HBM JESD22-A114A	4000	V
		MM JESD22-A115A	200	V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.

(2) All voltages are with respect to network ground terminal.

(3) The CJ4054 are guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the －40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical processcontrols.

(4) ESD testing is performed according to the respective JESD22 JEDEC standard.

The human body model is a 100 pF capacitor discharged through a 1.5kΩ resistor into each pin. The machine model is a 200pF capacitor discharged directly into each pin.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input voltage range(1)	V_{CC}	4.5	6.5	V
BAT Pin Output Current (Continuous)	I_{BAT}	10	600(2)	mA
Operating junction temperature range	T_J	0	70	°C
Fast-charge current programming resistor(3)	R_{PROG}	1.66	100	kΩ

(1) If V_{CC} is between UVLO and 4.5V, and above the battery voltage, then the IC is active (can deliver some charge to the battery), but the IC will have limited or degraded performance (some functions may not meet data sheet specifications). The battery may be undercharged (V_{FLOAT} less than in the specification), but will not be overcharged (V_{FLOAT} will not exceed specification).

(2) The thermal regulation feature reduces charge current if the IC's junction temperature reaches 120°C; thus without a good thermal design the maximum programmed charge current may not be reached.

(3) Use a 1% tolerance metal film resistor for R_{PROG} to avoid issues with the R_{PROG} short test when using the maximum charge current setting.

■ ELECTRICAL CHARACTERISTICS

Over recommended operating, T_J= 0~120°C range, typical values are tested at V_{CC}=5V and T_A=25°C, maximum and minimum values are guaranteed over 0°C to 70°C ambient temperature with a supply voltage in the range of 4.5V to 6.5V, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
POWER DOWN THRESHOLD – UNDERVOLTAGE LOCKOUT(UVLO)						
Undervoltage Lockout Threshold(1)	V_{UVL}	V_{CC} Rising : 0V→4V		3.9		V
Hysteresis on UVLO	ΔV_{UVL}	V_{CC} Falling: 4V→0V		150		mV
MANUAL SHUTDOWN						
Manual Shutdown Threshold Voltage	V_{MSD}	PROG Pin Rising	1.15	1.21	1.30	V
		PROG Pin Falling	0.9	1.0	1.1	V
QUIESCENT CURRENT						
Input Supply Current	$I_{CC(CHG)}$	Charge Mode(2), R_{PROG}=10kΩ		100	200	μA
	$I_{CC(STB)}$	Standby Mode (Charge Terminated)		25	50	μA
	$I_{CC(SHDN)}$	Shutdown Mode (R_{PROG} Not Connected or V_{CC}<V_{UVL})		25	50	μA
	$I_{CC(SLP)}$	Sleep Mode (V_{UVL} < V_{CC} < V_{BAT} + V_{SLP})		25	50	μA
Battery leakage current into BAT pin	$I_{BAT(STB)}$	Standby Mode (Charge Terminated), V_{BAT} = V_{FLOAT}		-2.5	-6.0	μA
	$I_{BAT(SHDN)}$	Shutdown Mode (R_{PROG} Not Connected or V_{CC}<V_{UVL})		±1	±2	μA
	$I_{BAT(SLP)}$	Sleep Mode (V_{UVL} < V_{CC} < V_{BAT} + V_{SLP} or V_{CC} Floating)		±1	±2	μA
VOLTAGE REGULATION, V_{CC}≥V_{FLOAT}+$V_{(DO-MAX)}$, I_{BAT}> I_{TERM}, CHARGER ENABLED, NO FAULT CONDITIONS DETECTED						
Regulated Output Voltage Accuracy	V_{FLOAT}	0°C ≦ T_A ≤ 85°C, I_{BAT} = 20mA, R_{PROG}=10kΩ	-50		+50	mV
Dropout voltage, V_{CC} – V_{BAT}	$V_{(DO)}$	I_{BAT}=600mA		240		mV
CURRENT REGULATION, V_{CC}≥V_{BAT}+$V_{(DO-MAX)}$, CHARGER ENABLED, NO FAULT CONDITIONS DETECTED						
Fast-Charge Current Range	I_{CHG}	V_{BAT} > V_{TRIKL}, I_{CHG}= K_{PROG} x V_{PROG} /R_{PROG}	10		600	mA
Fast-Charge Current Set Voltage	V_{PROG}	R_{PROG} = 10kΩ, Current Mode	0.9	1.0	1.1	V
Fast-Charge Current set factor	K_{PROG}	100mA≤I_{CHG}≤600mA $\frac{mA * k\Omega}{Volts}$		1000		
External resistor range	R_{PROG}	Resistor connected to PROG pin	1.66		100	kΩ
Fast-Charge Current in typical application		R_{PROG} = 2kΩ, V_{BAT}=4.0V Current Regulation Mode	450	500	550	mA
		R_{PROG} = 10kΩ, V_{BAT}=4.0V Current Regulation Mode	90	100	110	mA
PROG Pin Pull-Up Current	I_{PROG}			0.15		μA

(1) Specified by design, not production tested.

(2) Supply current includes PROG pin current (approximately 100μA) but does not include any current delivered to the battery through the BAT pin (approximately 100mA).

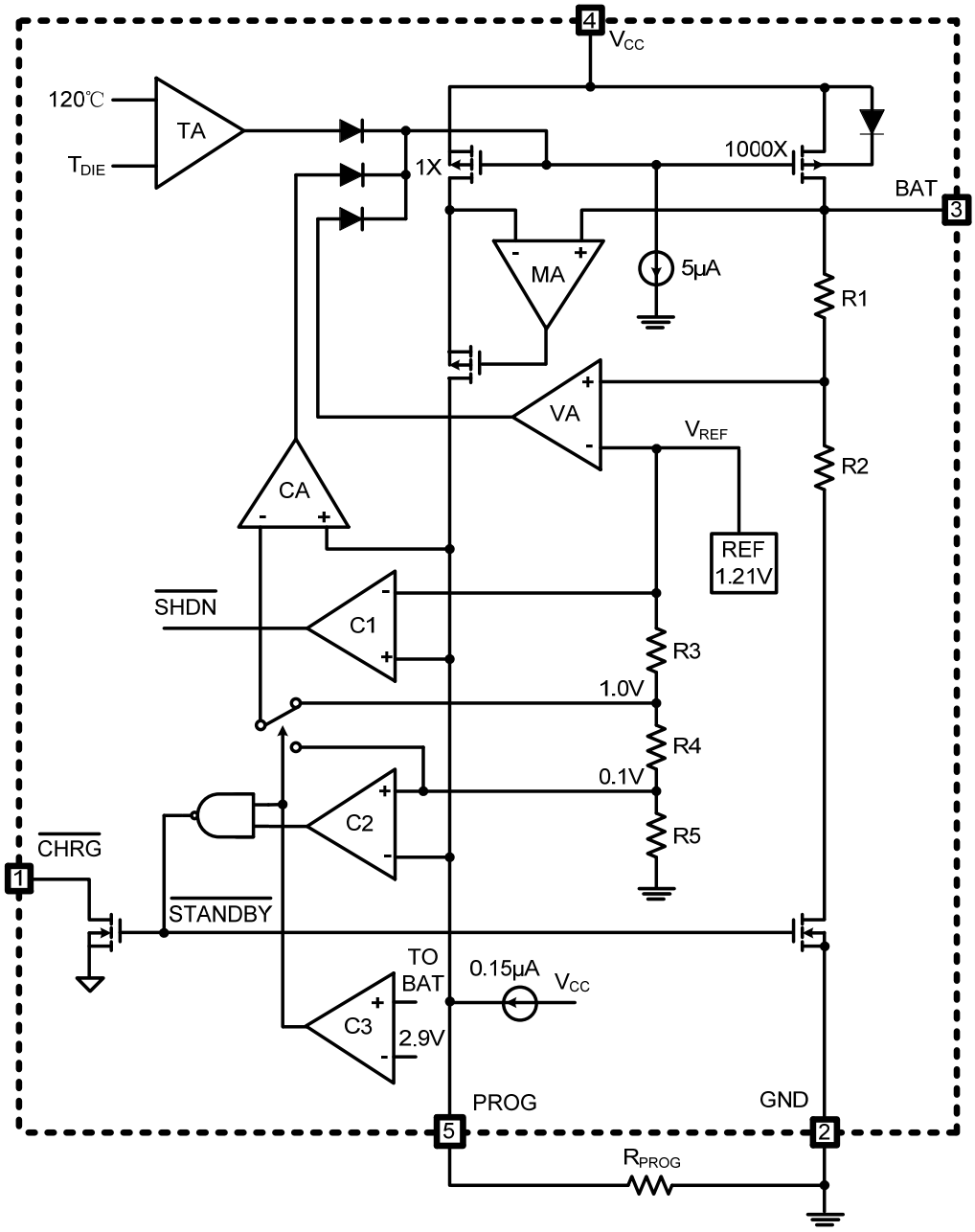
■ ELECTRICAL CHARACTERISTICS(continued)

Over recommended operating, T_J= 0~120°C range, typical values are tested at V_{CC}=5V and T_A=25°C, maximum and minimum values are guaranteed over 0°C to 70°C Ambient Temperature with a supply voltage in the range of 4.5V to 6.5V, unless otherwise noted.

PRE-CHARGE AND OUTPUT SHORT-CIRCUIT CURRENT REGULATION, V_{CC}–V_{BAT} > $V_{(DO-MAX)}$, V_{CC}≥4.5V, CHARGER ENABLED, NO FAULT CONDITIONS DETECTED; Thermal regulation loop not active						
Pre-charge to fast-charge transition threshold	V_{TRIKL}	R_{PROG} = 10kΩ, V_{BAT} Rising		2.9		V
Pre-charge Hysteresis	$V_{(TRIKL-HYS)}$	R_{PROG} = 10kΩ, V_{BAT} Falling		100		mV
Pre-charge Current range	$I_{(PRECHG)}$	V_{BAT} < V_{TRIKL}, $I_{(PRECHG)}$= K_{PROG} x V_{PRECHG} /R_{PROG}	0.3		70	mA
Pre-charge Current set voltage	V_{PRECHG}	Voltage on PROG pin, V_{BAT} < V_{TRIKL}		100		mV
Pre-charge Current in typical application		V_{BAT} < V_{TRIKL}, R_{PROG}=2kΩ		50		mA
Battery shorted regulation current	$I_{BAT(SHORT)}$	BAT=GND, R_{PROG}=2kΩ		50		mA
TEMPERATURE REGULATION (Thermal regulation), CHARGER ENABLED, NO FAULT CONDITIONS DETECTED						
Temperature regulation limit	$T_{J(REG)}$	V_{CC}= 5V, V_{BAT}=3.2 V, Fast-charge current set to 600mA		120		°C
CHARGE TERMINATION DETECTION, V_{BAT}= V_{FLOAT}, CHARGER ENABLED, NO FAULT CONDITIONS DETECTED, Thermal regulation LOOP NOT ACTIVE						
C/10 Charge termination detection current range	I_{TERM}(3)	V_{BAT} > V_{RECHG}, I_{TERM}= K_{PROG} x V_{TERM} /R_{PROG}	1		70	mA
C/10 Charge termination detection set voltage(4)	V_{TERM}	V_{BAT} > V_{RECHG}		100		mV
C/10 Charge termination detection in typical application		R_{PROG}=2kΩ		50		mA
		R_{PROG}=10kΩ	7	10	13	mA
Deglitch time, termination detected	$T_{DGL(TERM)}$	I_{BAT} Falling Below I_{CHG}/10	0.8	1.8	4	mS
BATTERY RECHARGE THRESHOLD						
Recharge Threshold Detection	△V_{RECHG}	V_{FLOAT}－V_{BAT} < △V_{RECHG}		150		mV
Deglitch time, recharge detection	$T_{DGL(RECHG)}$	V_{BAT} Falling	0.8	1.8	4.0	mS
SLEEP COMPARATOR						
Sleep mode entry threshold voltage	V_{SLP}	V_{CC} Falling, V_{UVL} < V_{BAT} ≤ V_{FLOAT}		80		mV
Sleep mode exit threshold voltage	$V_{(SLP_EXIT)}$	V_{CC} Rising , V_{UVL} < V_{BAT} ≤ V_{FLOAT}		100		mV
$\overline{CHRG}$ STATUS OUTPUT						
$\overline{CHRG}$ Pin Low-level Output Voltage	$V_{\overline{CHRG}}$	$I_{\overline{CHRG}}$=5mA (sink current)		0.3	0.6	V
SOFT START						
Soft-Start Time	t_{SS}	I_{BAT}=0 to I_{BAT} =1000V/R_{PROG}		20		μS

(3) I_{TERM} is expressed as a fraction of measured full charge current with indicated PROG resistor.
(4)The voltage on the PROG pin is compared to the V_{TERM} voltage to determine when the termination should occur.

■ BLOCK DIAGRAM



Future 2. Functional Block Diagram

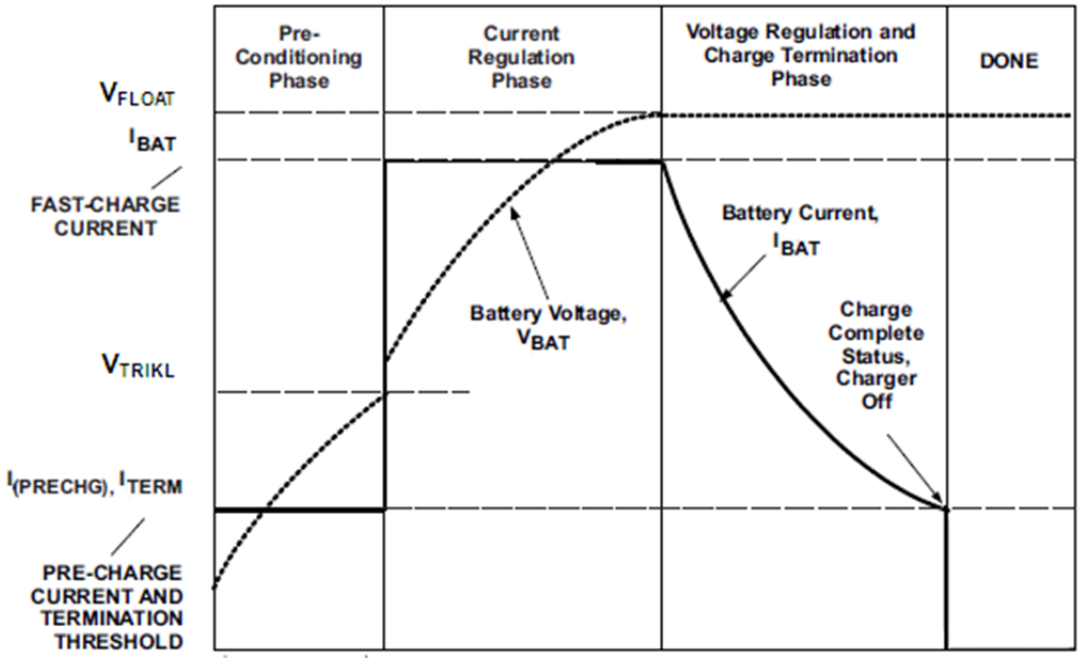
■ FUNCTIONAL DESCRIPTION

The CJ4054 series are highly integrated Li-Ion or Li-Pol linear battery chargers, targeted at space-limited portable applications. It operates from either a USB port or Wall Adapter and charges a single-cell Li-Ion or Li-Pol battery with up to 800mA of charge current.

The charge current is programmable using external components (R_{PROG} resistor). The charge process starts when an external input power is connected to the system, $V_{CC} > V_{UVL}$, $V_{CC} > V_{BAT} + V_{(SLP_EXIT)}$, the charger is enabled by the RPROG resistor connected and the battery voltage is below the recharge threshold, $V_{BAT} < V_{RECHG}$.

When the charger is enabled two control loops modulate the battery switch drain to source impedance to limit the BAT pin current to the programmed charge current value (charge current loop) or to regulate the BAT pin voltage to the programmed charge voltage value (charge voltage loop). If $V_{BAT} < V_{TRIKL}$ (2.9 V typical), the BAT pin current is internally set to 1/10th of the programmed fast-charge current value in current regulation mode.

A typical charge profile is shown below, for an operation condition that does not cause the IC junction temperature to exceed $T_{J(REG)}$ (120°C typical).



Future 3. Charging Profile With $T_{J(REG)}$

If the operating conditions cause the IC junction temperature to exceed $T_{J(REG),}$ the charge cycle is modified, with the activation of the integrated thermal control loop. The thermal control loop is activated when an internal voltage reference, which is inversely proportional to the IC junction temperature, is lower than a fixed, temperature stable internal voltage. The thermal loop overrides the other charger control loops and reduces the charge current until the IC junction temperature returns to $T_{J(REG)}$, effectively regulating the IC junction temperature.

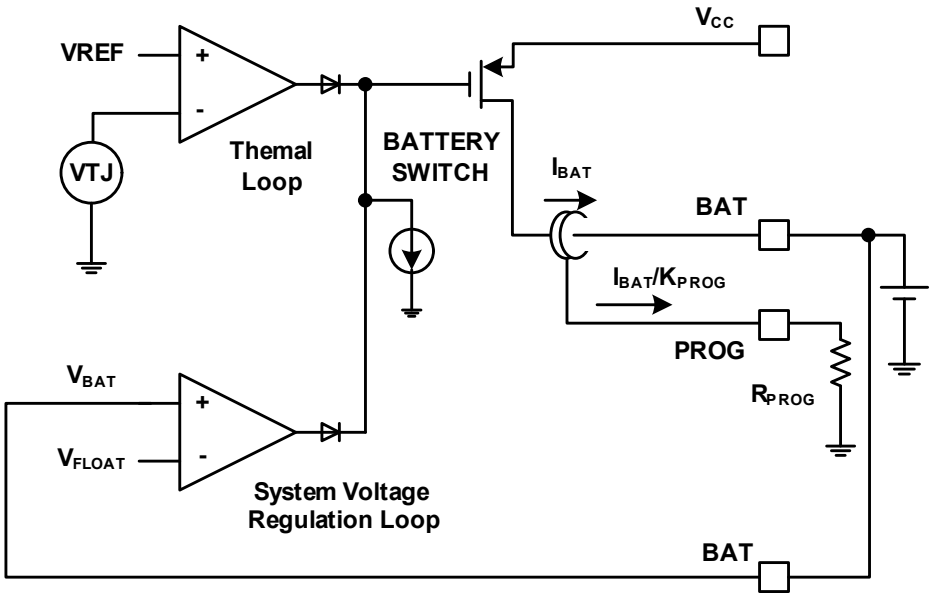


Figure 4. Thermal Regulation Circuit

A modified charge cycle, with the thermal loop active, is shown in Figure 5.

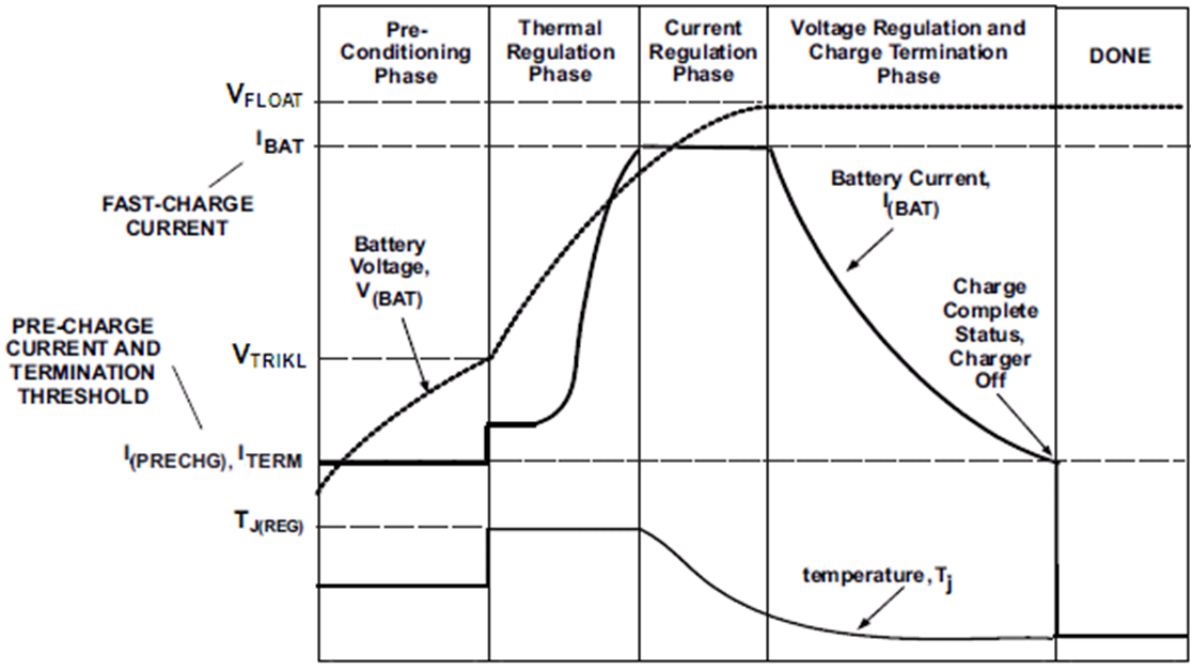


Figure 5. Charge Profile, Thermal Loop Active

■ OPERATING MODES

Power Down (Undervoltage Lockout, UVLO)

An internal undervoltage lockout circuit monitors the input voltage, the CJ4054 is in a power-down mode when the input power voltage (V_{CC}) is below the power-down threshold (Undervoltage Lockout threshold) VUVL. The UVLO circuit has a built-in hysteresis of 150mV.

During the power down mode, all IC functions are off. The integrated power MOSFET connected between V_{CC} and BAT pins is off, the status output pin CHRG is set to the high impedance state.

Sleep Mode

The CJ4054 enters the low-power sleep mode when the input power voltage (V_{CC}) is above the power down threshold (Undervoltage Lockout threshold) VUVL but still lower than the Sleep mode exit threshold, $V_{UVL} < V_{CC} < V_{BAT} + V_{(SLP_EXIT)}$. During the sleep mode, the charger is off. The integrated power MOSFET connected between VCC and BAT pins is off, the status output pin CHRG is set to the high impedance state.

The sleep mode is entered from any other state, if the input power (V_{CC}) is not detected. This feature prevents draining the battery during the absence of V_{CC}.

The backgate control circuit prevents any reverse current flowing from the battery to the adapter terminal during the charger off delay time.

Note that the $\overline{CHRG}$ pin is not deglitched, and it indicates input power loss immediately after the input voltage falls below the BAT pin voltage. If the input source frequently drops below the BAT pin voltage and recovers, a small capacitor can be used from $\overline{CHRG}$ to GND to prevent $\overline{CHRG}$ flashing events.

Begin Charge Mode

All blocks in the IC are powered up, and the CJ4054 is ready to start charging the battery. A new charge cycle is started when the control logic decides that all conditions required to enable a new charge cycle are met.

Charging Mode

When the charging mode is active, the CJ4054 executes the charging algorithm, as described in the operational flow chart, Figure 7.

Battery's absence Mode Operation

This mode is different than a typical LDO since it has different modes of operation, and delivers less current at lower output voltages.

Note that a load on the output prior to powering the device may keep the part in short-circuit mode. Also, during normal operation, exceeding the programmed fast-charge level causes the output to drop, further restricting the output power, and soon ends up in short-circuit mode. Operation with a battery or keeping the average load current below the programmed current level prevents this type of latch up.

NORMAL CHARGE CYCLE

A charge cycle begins when the voltage at the V_{CC} pin rises above the UVLO threshold level and a 1% program resistor is connected from the PROG pin to ground or when a battery is connected to the charger BAT pin. If the BAT pin voltage is less than the V_{TRIKL} threshold (2.9V typical), the charger enters pre-conditioning (trickle charge) mode. In this mode, the CJ4054 applies approximately 1/10th of the programmed fast-charge current value in current regulation mode to bring the battery voltage up to a safe level for full current charging.

When the BAT pin voltage rises above the V_{TRIKL} threshold (2.9V typical), the charger enters current regulation mode, where the programmed fast-charge current is applied to the battery. When the BAT pin approaches the final float voltage (V_{FLOAT}), the CJ4054 enters voltage regulation mode and the charge current begins to decrease. When the charge current drops to 1/10th of the programmed fast-charge current value in current regulation mode, the charge cycle ends.

PROGRAMMING CHARGE CURRENT

The charge current delivered to the battery from USB bus or wall adapter supply is programmed using a single resistor from the PROG pin to ground. The battery charge current is 1000 times the current out of the PROG pin. The program resistor and the charge current (ICHG) are calculated using the equations:

$I_{CHG} = K_{PROG} \times V_{PROG} / R_{PORG} = 1000V/R_{PORG}$

$R_{PORG} = K_{PROG} \times V_{PROG} / I_{CHG} = 1000V/I_{CHG}$

POWER ON RESET (POR)

The CJ4054 resets itself as the input voltage rises above the POR rising threshold. The CJ4054 has a typical rising POR threshold of 3.9V and a falling POR threshold of 3.75V. Then the charger begins to charge the battery.

LOW BATTERY CHARGE CONDITIONING (TRICKLE CHARGE)

During a charge cycle, if the BAT pin voltage is below the V_{TRIKL} threshold (2.9V typical), the CJ4054 applies a pre-charge current, $I(P_{RECHG})$, 1/10th of the programmed fast-charge current value in current regulation mode to the battery until the BAT pin voltage rises back above the V_{TRIKL} threshold (2.9V typical). This feature ensures that deeply discharged batteries are gradually charged before reapplying full charge current, to revive deeply discharged cells and decrease the power dissipation. The resistor connected between the PROG and GND, R_{PROG}, determines the pre-charge rate. The V_{PRECHG} and K_{PROG} parameters are specified in the specifications table.

$I_{(PRECHG)} = K_{PROG} \times V_{PRECHG} / R_{PROG} = 100V/R_{PROG}$

For example, if the charger is programmed to charge at 600mA from the wall adapter input and 500mA from the USB input, the charge current during pre-conditioning mode would be 60mA and 50mA, respectively.

BATTERY CURRENT REGULATION (FAST-CHARGE)

The CJ4054 offers on-chip current regulation. The current regulation is defined by the value of the resistor connected to PROG pin.

During a charge cycle, the fast-charge current ICHG is applied to the battery if the BAT pin voltage is above the V_{TRIKL} threshold (2.9V typical):

$I_{CHG} = K_{PROG} \times V_{PROG} / R_{PROG} = 1000V/R_{PROG}$

Where KPROG is the BAT pin output current set factor and VPROG is the BAT pin output current set voltage.

BATTERY VOLTAGE REGULATION

Voltage regulation feedback is accomplished through the BAT pin. The battery pack voltage is sensed through the BAT pin, which is tied directly to the positive side of the battery pack. The CJ4054 monitors

the battery pack voltage between the BAT and GND pins. When the battery voltage rises to V_{FLOAT} threshold, the voltage regulation phase begins and the charging current begins to taper down. The voltage regulation threshold V_{FLOAT} is fixed by an internal IC voltage reference.

MONITORING CHARGE CURRENT

When the charge function is enabled internal circuits generate a current proportional to the charge current at the PROG pin. This current, when applied to the external charge current programming resistor R_{PROG} generates an analog voltage that can be monitored by an external host to calculate the current sourced from the BAT pin. Charge current out of the BAT pin can be determined at any time by monitoring the PROG pin voltage and using the following equations:

$V_{PROG} = I_{BAT} \times R_{PROG} / K_{PROG} = I_{BAT} \times R_{PROG} /1000$

CHARGE TERMINATION DETECTION

The charging current is monitored during the voltage regulation phase. Charge termination is indicated at the $\overline{CHRG}$ pin ($\overline{CHRG}$=High-Z) once the charge current falls below the termination current threshold ITERM after the final float voltage is reached:

$I_{TERM} = K_{PROG} \times V_{TERM} / R_{PROG} = 100V/R_{PROG}$

which is 1/10th of the programmed fast-charge current value in current regulation mode.

This condition is detected by using an internal, filtered comparator to monitor the PROG pin. When the PROG pin voltage falls below 100mV **(Note: Any external sources that hold the PROG pin above 100mV will prevent the CJ4054 from terminating a charge cycle.)** for longer than $T_{DGL(TERM)}$ (1.8ms typical), charging is terminated. The charge current is latched off and the CJ4054 enters charge done mode, where the input supply current drops to 50A. **(Note: C/10 charge termination is disabled in trickle charging and thermal regulation modes.)**

When charging, transient loads on the BAT pin can cause the PROG pin to fall below 100mV for short periods of time before the DC charge current has dropped to 1/10th of the programmed fast-charge current value in current regulation mode. The 1.8ms deglitch period ($T_{DGL(TERM)}$) on the termination comparator ensures that transient loads of this nature do not result in premature charge cycle termination and false termination indication. Once the average charge current drops below 1/10th the programmed fast-charge current value in current regulation mode, the CJ4054 terminates the charge cycle and ceases to provide any current through the BAT pin. In this state, all loads on the BAT pin must be supplied by the battery.

The CJ4054 constantly monitors the BAT pin voltage in charge done mode. If this voltage drops below the recharge threshold (V_{RECHG}), another charge cycle begins and current is once again supplied to the battery. Table 2 describes the termination latch functionality.

Table 2. Termination Latch Functionality

TERMINATION DETECTED LATCHED WHEN	TERMINATION LATCH RESET AT
$I_{BAT} < I_{TERM}$ **AND** $t > T_{DGL(TERM)}$ **AND** $V_{BAT} > V_{RECHG}$	New charging cycle started; see state machine diagram

CHARGE STATUS INDICATOR ($\overline{CHRG}$)

The charge status output has two different states: strong pull-down (~10mA) and high impedance. The strong pull-down state indicates that the CJ4054 is in a charge cycle. Once the charge cycle has

terminated, the pin state is set to high impedance. High impedance may also indicate that the CJ4054 is in undervoltage lockout mode: either V_{CC} is less than 100mV above the BAT pin voltage or insufficient voltage is applied to the V_{CC} pin. A microprocessor can be used to distinguish between the two states—this method is discussed in the Applications Information section.

THERMAL REGULATION LOOP

An internal thermal feedback loop reduces the programmed charge current if the die temperature attempts to rise above a preset value of approximately 120°C. This feature protects the CJ4054 from excessive temperature and allows the user to push the limits of the power handling capability of a given circuit board without risk of damaging the CJ4054. The charge current can be set according to typical (not worst-case) ambient temperatures with the assurance that the charger will automatically reduce the current in worst-case conditions.

OVER-CURRENT PROTECTION

Over-current protection is provided in all modes of operation, including voltage regulation. The output current is limited to either the programmed pre-charge current limit value or the fast-charge current limit value, depending on the voltage at the output.

MANUAL SHUTDOWN

At any point in the charge cycle, the CJ4054 can be put into shutdown mode by removing RPROG thus floating the PROG pin. This reduces the battery drain current to less than 2 A and the supply current to less than 25 A. A new charge cycle can be initiated by reconnecting the program resistor. In manual shutdown, The CHRG pin is in a high impedance state.

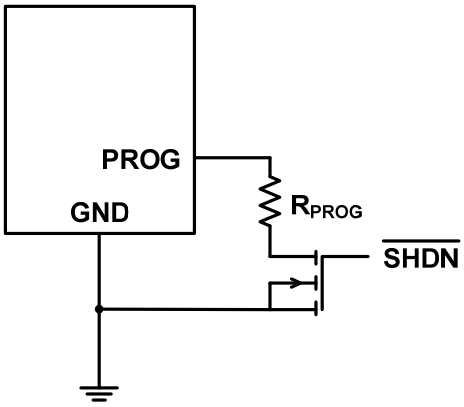


Figure 6. Shutdown Operation

RECHARGE

Once the charge cycle is terminated, the charger sits idle and continuously monitors the voltage on the BAT pin using a comparator with a 1.8ms filter time, $T_{DGL(RECHG)}$. A charge cycle automatically restarts when the battery voltage falls below VRECHG threshold (which corresponds to approximately 80%-90% battery capacity). This ensures that the battery is kept at, or near, a fully charged condition and eliminates the need for periodic charge cycle initiations. $\overline{CHRG}$ output enters a strong pull-down state during recharge cycles.

If the battery is removed from the charger, a sawtooth waveform of approximately 100mV appears at the battery output. This is caused by the repeated cycling between termination and recharge events. This cycling results in pulsing at the $\overline{CHRG}$ output; an LED connected to this pin will exhibit a blinking pattern, indicating to the user that a battery is not present. The frequency of the sawtooth is dependent on the

amount of output capacitance. See the Battery Absent Detection section for additional details.

STATE MACHINE DIAGRAM

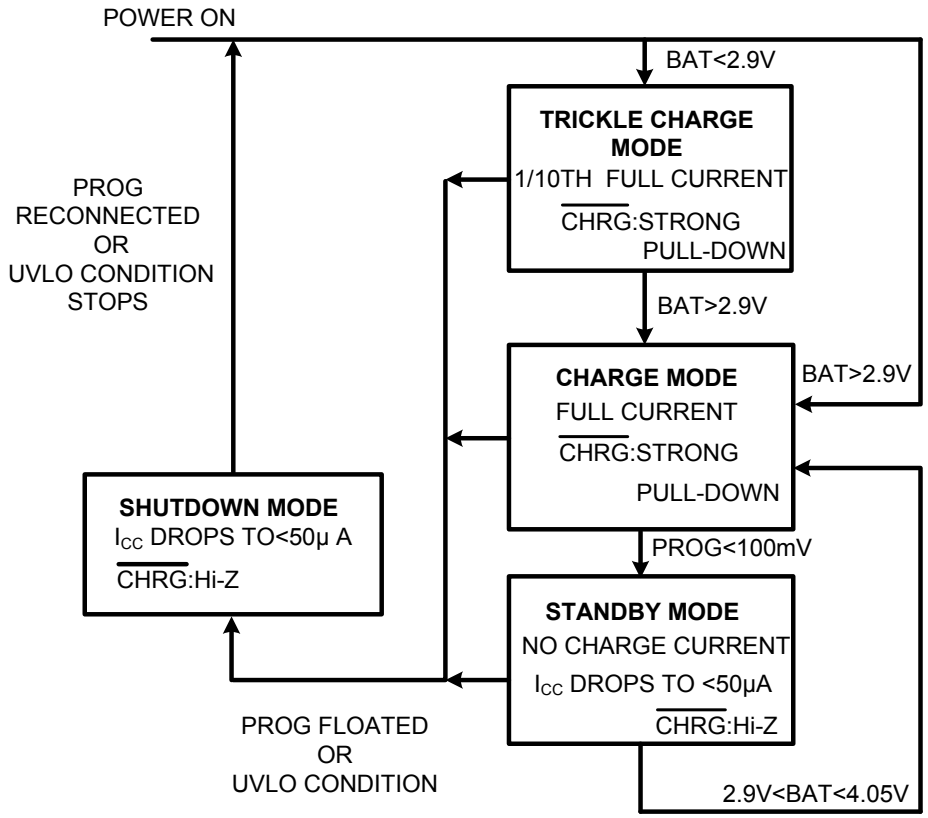


Figure 7. Operational Flow Chart

■ APPLICATION INFORMATIONS

STABILITY CONSIDERATIONS

The constant-voltage mode feedback loop is stable without an output capacitor provided a battery is connected to the charger output. With no battery present, an output capacitor is recommended to reduce ripple voltage. When using high value, low ESR ceramic capacitors, it is recommended to add a 1Ω resistor in series with the capacitor. No series resistor is needed if tantalum capacitors are used.

In constant-current mode, the PROG pin is in the feedback loop, not the battery. The constant-current mode stability is affected by the impedance at the PROG pin. With no additional capacitance on the PROG pin, the charger is stable with program resistor values as high as 20k. However, additional capacitance on this node reduces the maximum allowed program resistor. The pole frequency at the PROG pin should be kept above 100kHz. Therefore, if the PROG pin is loaded with a capacitance, C_{PROG}, the following equation can be used to calculate the maximum resistance value for R_{PROG}:

$$R_{PROG} \leq \frac{1}{2\pi \times 10^5 \times C_{PROG}}$$

Average, rather than instantaneous, charge current may be of interest to the user. For example, if a switching power supply operating in low current mode is connected in parallel with the battery, the average current being pulled out of the BAT pin is typically of more interest than the instantaneous current pulses.

In such a case, a simple RC filter can be used on the PROG pin to measure the average battery current as shown in Figure 8. A 10k resistor has been added between the PROG pin and the filter capacitor to ensure stability.

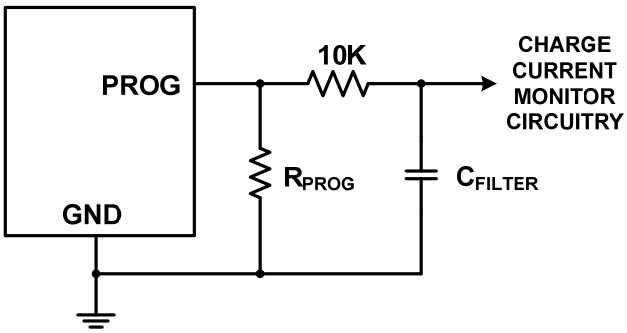


Figure 8. Isolating Capacitive Load on PROG Pin and Filtering

POWER DISSIPATION

The conditions that cause the CJ4054 to reduce charge current through thermal feedback can be approximated by considering the power dissipated in the IC. Nearly all of this power dissipation is generated by the internal MOSFET this is calculated to be approximately:

$P_D = (V_{CC} – V_{BAT}) • I_{BAT}$

where P_D is the power dissipated, V_{CC} is the input supply voltage, V_{BAT} is the battery voltage and I_{BAT} is the charge current. The approximate ambient temperature at which the thermal feedback begins to protect the IC is:

$T_A = 120°C – P_D\theta_{JA}$

$T_A = 120°C – (V_{CC} – V_{BAT}) • I_{BAT} • \theta_{JA}$

Example: An CJ4054 operating from a 5V USB supply is programmed to supply 400mA full-scale current to a discharged Li-Ion battery with a voltage of 3.75V. Assuming θ_{JA} of SOT-23-5L is 150°C/W (see Board Layout Considerations), the ambient temperature at which the CJ4054 will begin to reduce the charge current is approximately:

$T_A = 120°C – (5V – 3.75V) • 400mA • 150°C/W$

$T_A = 120°C – 0.5W • 150°C/W = 120°C –75°C$

$T_A = 45°C$

The CJ4054 can be used above 45°C ambient, but the charge current will be reduced from 400mA. The approximate current at a given ambient temperature can be approximated by:

$$I_{BAT} = \frac{120℃ - T_A}{(V_{CC} - V_{BAT}) \times \theta_{JA}}$$

Using the previous example with an ambient temperature of 60°C, the charge current will be reduced to approximately:

$$I_{BAT} = \frac{120℃ - 60℃}{(5V - 3.75V) \times 150℃/W} = \frac{60℃}{187.5℃/A}$$

$$I_{BAT} = 320mA$$

Moreover, when thermal feedback reduces the charge current, the voltage at the PROG pin is also reduced proportionally as discussed in the Operation section.

It is important to remember that CJ4054 applications do not need to be designed for worst-case thermal conditions since the IC will automatically reduce power dissipation when the junction temperature reaches approximately 120°C.

THERMAL CONSIDERATIONS

Because of the small size of the SOT package, it is very important to use a good thermal PC board layout to maximize the available charge current. The thermal path for the heat generated by the IC is from the die to the copper lead frame, through the package leads, **(especially the ground lead)** to the PC board copper. The PC board copper is the heat sink. The footprint copper pads should be as wide as possible and expand out to larger copper areas to spread and dissipate the heat to the surrounding ambient. Feedthrough vias to inner or backside copper layers are also useful in improving the overall thermal performance of the charger. Other heat sources on the board, not related to the charger, must also be considered when designing a PC board layout because they will affect overall temperature rise and the maximum charge current

The following table lists thermal resistance for several different board sizes and copper areas. All measurements were taken in still air on 3/32" FR-4 board with the device mounted on topside.

Table 3. Measured Thermal Resistance (2-Layer Board*)

COPPER AREA		BOARD AREA	THERMAL RESISTANCE JUNCTION-TO-AMBIENT
TOPSIDE	BACKSIDE		
2500mm^2	2500mm^2	2500mm^2	125°C/W
1000mm^2	2500mm^2	2500mm^2	125°C/W
225mm^2	2500mm^2	2500mm^2	130°C/W
100mm^2	2500mm^2	2500mm^2	135°C/W
50mm^2	2500mm^2	2500mm^2	150°C/W

***Each layer uses one ounce copper**

Table 4. Measured Thermal Resistance (4-Layer Board)**

COPPER AREA (EACH SIDE)	BOARD AREA	THERMAL RESISTANCE JUNCTION-TO-AMBIENT
2500mm^2	2500mm^2	80°C/W

***Top and bottom layers use two ounce copper, inner layers use one ounce copper.**

****10,000mm^2 total copper area**

INCREASING THERMAL REGULATON CURRENT

Reducing the voltage drop across the internal MOSFET can significantly decrease the power dissipation in the IC. This has the effect of increasing the current delivered to the battery during thermal regulation. One method is by dissipating some of the power through an external component, such as a resistor or diode.

Example: An CJ4054 operating from a 5V wall adapter is programmed to supply 800mA full-scale current to a discharged Li-Ion battery with a voltage of 3.75V. Assuming θ_{JA} is 125°C/W, the approximate charge current at an ambient temperature of 25°C is:

$$I_{BAT} = \frac{120℃ - 25℃}{(5V - 3.75V) \times 125℃/W} = 608mA$$

By dropping voltage across a resistor in series with a 5V wall adapter (shown in Figure 9), the on-chip power dissipation can be decreased, thus increasing the thermally regulated charge current

$$I_{BAT} = \frac{120℃ - 25℃}{(V_S - I_{BAT}R_{CC} - V_{BAT}) \times \theta_{JA}}$$

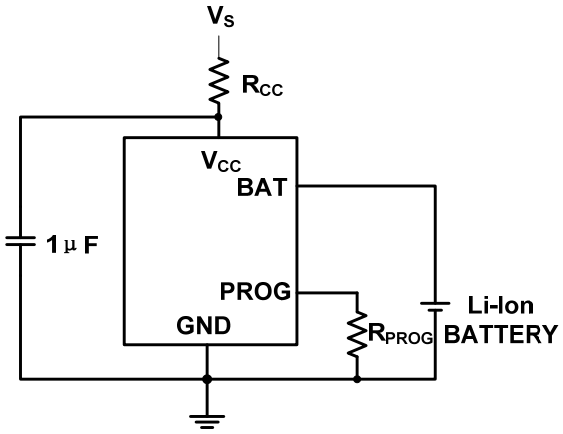


Figure 9. A Circuit to Maximize Thermal Mode Charge Current

Solving for I_{BAT} using the quadratic formula **(Note: Large values of R_{CC} will result in no solution for I_{BAT}. This indicates that the CJ4054 will not generate enough heat to require thermal regulation)**.

$$I_{BAT} = \frac{(V_S - V_{BAT}) - \sqrt{(V_S - V_{BAT})^2 - \frac{4R_{CC}(120℃ - T_A)}{\theta_{JA}}}}{2R_{CC}}$$

Using R_{CC}=0.25Ω, V_S=5V, V_{BAT}=3.75V, T_A=25°C and θ_{JA}=125°C/W we can calculate the thermally regulated charge current to be: I_{BAT}=708.4mA

While this application delivers more energy to the battery and reduces charge time in thermal mode, it may actually lengthen charge time in voltage mode if V_{CC} becomes low enough to put the CJ4054 into dropout.

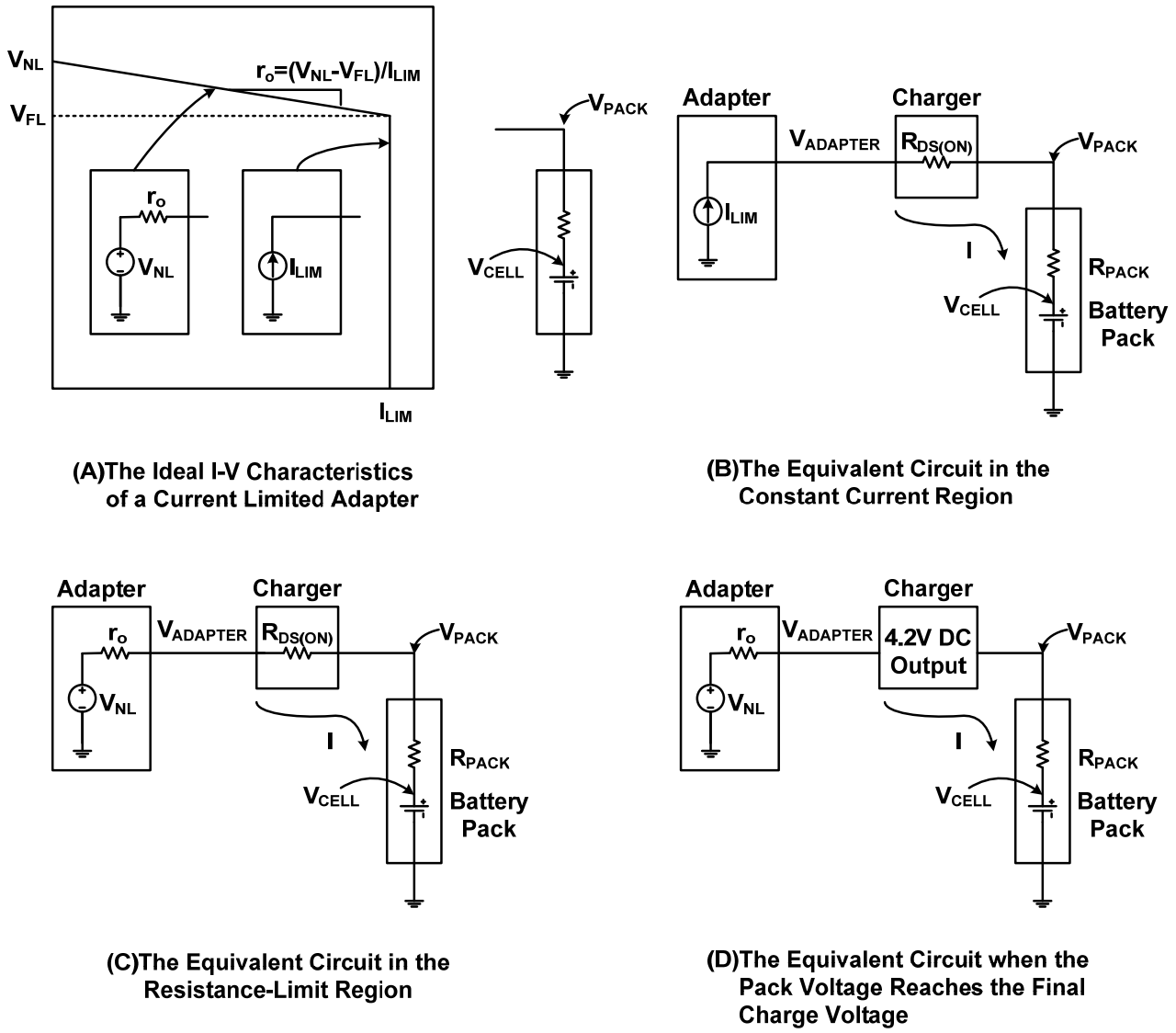
This technique works best when R_{CC} values are minimized to keep component size small and avoid dropout. Remember to choose a resistor with adequate power handling capability.

Operating a Charging Adapter in Current Limit

In high charging current applications, charger power dissipation can be greatly reduced by operating the charging adapter in current limit. The CJ4054 supports adapter current- limited charging with a low UVLO falling threshold and with internal circuitry designed for low input voltage operation. To operate an adapter in current limit, R_{PROG} is chosen such that the programmed fast-charge current I_{CHG} exceeds the current limit of the charging adapter I_{LIM}.

Figure 10 shows the ideal current-voltage characteristics of a current-limited adapter. V_{NL} is the no-load adapter output voltage and V_{FL} is the full load voltage at the current limit I_{LIM}. Before its output current reaches the limit I_{LIM}, the adapter presents the characteristics of a voltage source. The slope r_O represents the output resistance of the voltage supply. For a well regulated supply, the output resistance can be very small, but some adapters naturally have a certain amount of output resistance.

The adapter is equivalent to a current source when running in the constant-current region. Being a current source, its output voltage is dependent on the load, which, in this case, is the charger and the battery.



(A)The Ideal I-V Characteristics of a Current Limited Adapter

(B)The Equivalent Circuit in the Constant Current Region

(C)The Equivalent Circuit in the Resistance-Limit Region

(D)The Equivalent Circuit when the Pack Voltage Reaches the Final Charge Voltage

Figure 10. The Equivalent Circuit of the Charging System Working with Current Limited Adapter

Note that if I_{LIM} is less than 10% of I_{CHG}, then the adapter voltage can be pulled down to the battery voltage while the battery voltage is below the pre-charge threshold. In this case, care must be taken to ensure that the adapter will maintain its current limit below 10% of I_{CHG} at least until the battery voltage exceeds the pre-charge threshold. Failure to do so could permit charge current to exceed the pre-charge current while the battery voltage is below the pre-charge threshold. This happens because the low input voltage will also compress the pre-charge threshold internal reference voltage to below the battery voltage. This will prematurely advance the charger logic from pre-charge current regulation to fast-charge regulation, and the charge current will exceed the safe level recommended for pre-charge conditioning. The low UVLO falling threshold (V_{UVL-F}) permits the adapter voltage to be pulled down to just above the battery voltage by the charging load whenever the adapter current limit is less than the programmed fast -charge current. The CJ4054 should be operated with adapter voltage below the rising selection threshold (V_{UVL}) only if the low input voltage is the result of adapter current limiting. This implies that the V_{CC} pin first exceeds V_{UVL} to begin charging, and is subsequently pulled down to just above the battery voltage by the charging load.

Interaction of Thermal Limiting and Current Limited Adapter Charging

To permit the charge current to be limited by the adapter, it is necessary that the fast-charge current be programmed greater than the maximum adapter current, (I_{LIM}). In this configuration, the CC regulator will operate with its pass device fully on (in saturation, also called “dropout”). The voltage drop from V_{CC} to BAT is determined by the product of the minimum R_{DS-ON} of the pass device multiplied by the adapter supply current.

In dropout, the power dissipation in the CJ4054 is P_{ILIM} = (minimum R_{DS-ON}) x $(I_{LIM})^2$. Since minimum R_{DS-ON} does not vary with battery voltage, dropout power dissipation is constant throughout the CC portion of the charge cycle while the adapter remains in current limit. The CJ4054 junction temperature will rise above ambient by P_{ILIM} x θ_{JA}. If the device temperature rises to the temperature at which the temperature limit regulation control loop limits charging current (rather than the current being limited by the adapter), the input voltage will rise to the adapter regulation voltage. The power dissipation will increase so that the temperature limit regulation will further limit charge current. This will keep the adapter in voltage regulation for the remainder of the charge cycle. In this case, the CJ4054 will continue to charge with thermal limiting until charge current decreases while in CV regulation (reducing power dissipation sufficiently). This results in a slow charge cycle, but with no other negative effect.

To ensure that the adapter remains in current limit, the internal device temperature must not rise to $T_{J(REG)}$. This implies that θ_{JA} must be kept small enough, through careful layout, to ensure that:

$$T_J = T_A + (P_{ILIM} \times \theta_{JA}) < T_{J(REG)}$$

SELECTING INPUT V_{CC} BYPASS CAPACITOR

In most applications, all that is needed is a bypass capacitor, typically a 4.7 F capacitor placed in close proximity to VCC and GND pins, works well. The CJ4054 is designed to work with both regulated and unregulated external dc supplies. If a non-regulated supply is chosen, the supply unit should have enough capacitance to hold up the supply voltage to the minimum required input voltage at maximum load. If not, more capacitance has to be added to the input of the charger.

A 4.7 F chip ceramic capacitor is recommended for the input bypass capacitor, because it provides low ESR and ESL and can handle the high RMS ripple currents. However, some high Q capacitors may produce high transients due to self-resonance under some start-up conditions, such as connecting the charger input to a hot power source. Adding a 1Ω resistor in series with an X5R ceramic capacitor will minimize start-up voltage transients.

Protecting the V_{CC} Pin from Overvoltage Transients

Many types of capacitors can be used for input bypassing, however, caution must be exercised when using multilayer ceramic capacitors to bypass the V_{CC} pin, which powered by USB bus or Wall Adapter Input. High voltage transients can be generated under some start-up conditions, depending on the power supply characteristics and cable length, such as when the USB or wall adapter is hot plugged. When power is supplied via the USB bus or wall adapter, the cable inductance along with the self resonant and high Q characteristics of some types of ceramic capacitors can cause substantial ringing which could exceed the maximum voltage pin ratings and damage the CJ4054. The long cable lengths of most wall adapters and USB cables makes them especially susceptible to this problem. To bypass the V_{CC} pin, add a 1Ω resistor in series with an X5R ceramic capacitor to lower the effective Q of the network and greatly reduce the ringing. A tantalum, OS-CON, or electrolytic capacitor can be used in place of the ceramic and resistor, as their higher ESR reduces the Q, thus reducing the voltage ringing.

The oscilloscope photograph in Figure 11 shows how serious the overvoltage transient can be for the

USB and wall adapter inputs. For both traces, a 5V supply is hot-plugged using a three foot long cable. For the top trace, only a 4.7µF capacitor (without the recommended 1Ω series resistor) is used to locally bypass the input. This trace shows excessive ringing when the 5V cable is inserted, with the overvoltage spike reaching 10V. For the bottom trace, a 1Ω resistor is added in series with the 4.7µF capacitor to locally bypass the 5V input. This trace shows the clean response resulting from the addition of the 1Ω resistor.

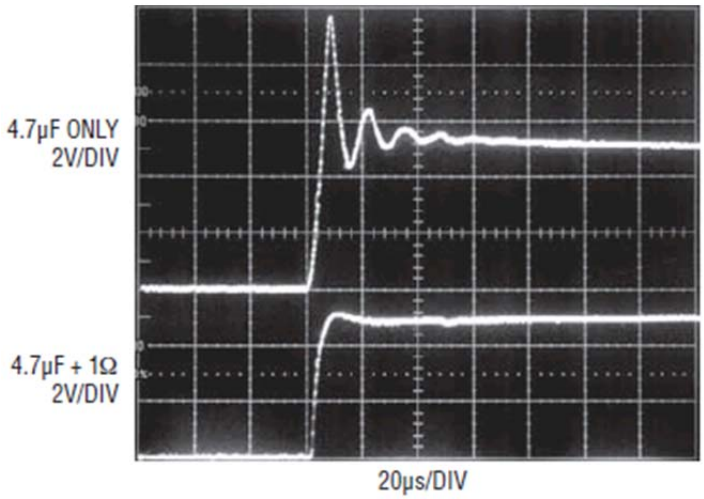


Figure 11. Waveforms Resulting from Hot-Plugging a 5V Input Supply

Even with the additional 1Ω resistor, bad design techniques and poor board layout can often make the overvoltage problem even worse. System designers often add extra inductance in series with input lines in an attempt to minimize the noise fed back to those inputs by the application. In reality, adding these extra inductances only makes the overvoltage transients worse. Since cable inductance is one of the fundamental causes of the excessive ringing, adding a series ferrite bead or inductor increases the effective cable inductance, making the problem even worse. For this reason, **do not** add additional inductance (ferrite beads or inductors) in series with the USB or wall adapter inputs. For the most robust solution, 6V transorbs or zener diodes may also be added to further protect the USB and wall adapter inputs. Two possible protection devices are the SM2T from ST Microelectronics and the EDZ series devices from ROHM.

Always use an oscilloscope to check the voltage waveforms at the V_{CC} pin during USB and wall adapter hot-plug events to ensure that overvoltage transients have been adequately removed.

USB Inrush Limiting

When a USB cable is plugged into a portable product, the inductance of the cable and the high-Q ceramic input capacitor form an L-C resonant circuit. If the cable does not have adequate mutual coupling or if there is not much impedance in the cable, it is possible for the voltage at the input of the product to reach as high as twice the USB voltage (~10V) before it settles out. In fact, due to the high voltage coefficient of many ceramic capacitors (a nonlinearity), the voltage may even exceed twice the USB voltage. To prevent excessive voltage from damaging the CJ4054 during a hot insertion, it is best to have a low voltage coefficient capacitor at the V_{CC} pin to the CJ4054 family. This is achievable by selecting an MLCC capacitor that has a higher voltage rating than that required for the application. For example, a 16V, X5R, 10µF capacitor in a 1206 case would be a better choice than a 6.3V, X5R, 10µF capacitor in a smaller 0805 case.

Alternatively, the following soft connect circuit in Figure 12 can be employed. In this circuit, capacitor C2

holds MN1 off when the cable is first connected. Eventually C2 begins to charge up to the USB input voltage applying increasing gate support to MN1. The long time constant of R1 and C2 prevent the current from building up in the cable too fast thus dampening out any resonant overshoot.

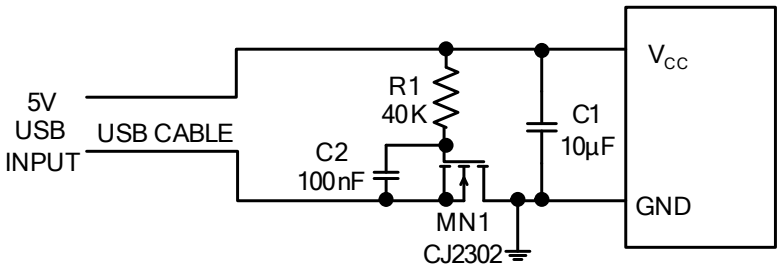


Figure 12. USB Soft Connect Circuit

CHARGE CURRENT SOFT-START and SOFT-STOP

The CJ4054 includes a soft-start circuit to minimize the inrush current at the start of a charge cycle. When a charge cycle is initiated, the charge current ramps from zero to the full-scale current over a period of approximately 20µs. During charger soft-start, the CJ4054 ramps up the voltage on PROG pin with constant well-controlled slew rate. The charging current is proportional to the PROG voltage. Likewise, internal circuitry slowly ramps the charge current from full-scale to zero when the charger is shut off or self terminates. This has the effect of minimizing the transient current load on the power supply during start-up and charge termination.

CHARGE CYCLE STATUS OUTPUT

$\overline{\text{CHRG}}$ pin is internally connected to an N-channel open drain MOSFET. The CJ4054 family provides battery charge status via $\overline{\text{CHRG}}$ status pin.

The open drain status output that is not used should be tied to ground.

The following table lists the indicator status and its corresponding charging state.

Table 5. Charge Status Indicator(1)

Charge State Description	$\overline{\text{CHRG}}$
Preconditioning-Current Mode (Trickle) Charge	ON
Constant-Current Mode (Fast) Charge	ON
Constant-Voltage Mode (Taper) Charge, $I_{BAT}>I_{TERM}$	ON
Charge Temination ($I_{BAT}<I_{TERM}$, Charge Done)	HI-Z
Power Down (Undervoltage Lockout) Mode	HI-Z
Sleep Mode ($V_{UVL}<V_{CC}< V_{BAT} + V_{(SLP_EXIT)}$, or the V_{CC} is removed)	HI-Z
Shutdown Mode(PROG pin floating)	HI-Z
No battery with Charge Enabled	FLASH Rate depends on C_{BAT}
Fault Condition (Battery Short Circuit)	ON

(1) Pulse loading on the BAT pin may cause the IC to cycle between Done and charging states (LEDs Flashing)

The $\overline{\text{CHRG}}$ status pin can be used to communicate to the host processor or drive LEDs.
It is supposed that a red LED or a green LED are connected to $\overline{\text{CHRG}}$ pin
The LEDs should be biased with as little current as necessary to create reasonable illumination, therefore,

a ballast resistor should be placed between the LED cathode and the status pin. LED current consumption will add to the overall thermal power budget for the device package, hence it is good to keep the LED drive current to a minimum 2mA should be sufficient to drive most low cost red or green LEDs. It is not recommended to exceed 10mA for driving an individual status LED. The required ballast resistor values can be estimated using following formula:

$R_{BALLAST} = [V_{CC} - V_{F(LED)}] / I_{LED}$

Example:

$R_{BALLAST} = [5.0V - 2.0V] / 2mA = 1.5k\Omega$

Note: Red LED forward voltage (V_F) is typically 2.0V@ 2mA.

$\overline{\text{CHRG}}$ STATUS OUTPUT Pin

When a discharged battery is connected to the charger, the constant current portion of the charge cycle begins and the $\overline{\text{CHRG}}$ pin pulls to ground. The $\overline{\text{CHRG}}$ pin can sink up to 10mA to drive an LED that indicates that a charge cycle is in progress.

When the battery is nearing full charge, the charger enters the constant-voltage portion of the charge cycle and the charge current begins to drop. When the charge current drops below 1/10 of the programmed current, the charge cycle ends and the strong pull-down is replaced by the high impedance, indicating that the charge cycle has ended. If the input voltage is removed or drops below the undervoltage lockout threshold, the $\overline{\text{CHRG}}$ pin becomes high impedance. Figure 13 shows that by using a pull-up resistor, a microprocessor can detect all two states from this pin.

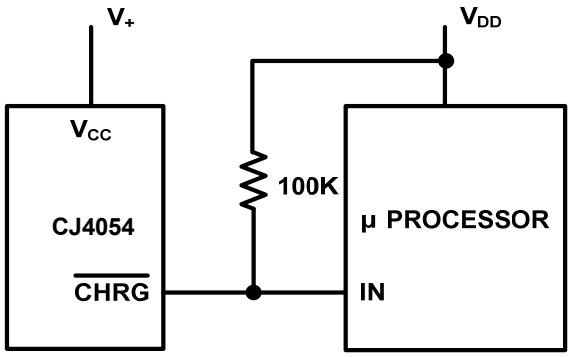


Figure 13. Using a Microprocessor to Determine $\overline{\text{CHRG}}$ State

BATTERY ABSENT DETECTION

The CJ4054 provides a battery absent detection scheme to reliably detect insertion and/or removal of battery packs.

If the battery is not present, the charger will charge the output capacitor to the regulation voltage quickly, then the BAT pin's voltage decays slowly to recharge threshold because of low leakage current at BAT pin, which results in a 100mV ripple waveform at BAT pin, in the meantime, CHRG pin outputs a pulse to indicate that the battery's absence. The pulse's frequency is around 1Hz when a 10µF output capacitor is used.

REVERSE POLARITY INPUT VOLTAGE PROTECTION

In some applications, protection from reverse polarity voltage on V_{CC} is desired. If the supply voltage is high enough, a series blocking diode can be used. In other cases, where the voltage drop must be kept low a P-channel MOSFET can be used (as shown in Figure 14).

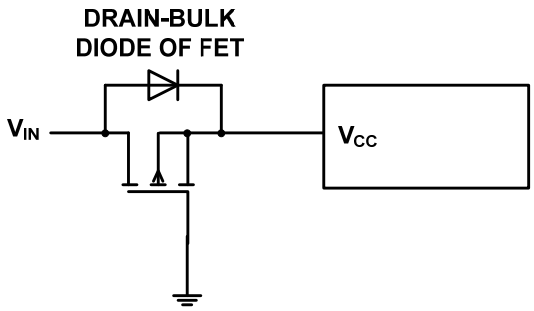


Figure 14. Low Loss Input Reverse Polarity Protection

Dynamically Selectable Charge Current

The PROG resistance can be altered dynamically under processor control by switching a second PROG pin resistor. When the higher current is required, the switch is turned on, making the effective programming resistance equal to the parallel combination of the two resistors. The external circuit is illustrated in Figure 15.

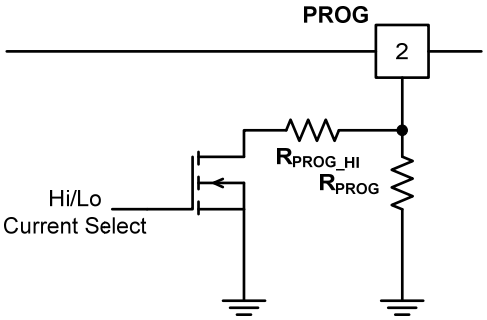


Figure 15. Dynamic selection of low and high charge currents

Note that the PROG pin resistor programs the fast-charge, pre-charge, and termination currents, so all will be modified by a change in the PROG pin resistor.

An open-drain GPIO can be used directly to engage the parallel resistor R_{PROG_HI}. Care must be taken to ensure that the R_{DS-ON} of the GPIO is considered in the selection of R_{PROG_HI}. Also important is the part-to-part and temperature variation of the GPIO R_{DS-ON}, and their contribution to the High Current charge current tolerance. A small amount of current could, potentially, flow from PROG into the GPIO ESD structure through R_{PROG_HI} during this event. While unlikely to do any harm, this effect must also be considered.

USB Dedicated Charger Compatibility

The CJ4054 is well suited to the USB Charging Specification, Revision 1.0, Dedicated Charger, Sections 3.5 and 4.1, due to thermal limiting and its current-limited-supply charging behavior.

The USB Dedicated Charger is required to limit its output current to more than 0.5A and less than 1.5A. A dedicated charger identifies itself by shorting together the USB D+ and D- lines. Once the dedicated charger is detected, the CJ4054, with its 800mA maximum programmed fast-charge current, permits the fast-charge current to be set higher than the 500mA USB High Power Mode specified limit to permit faster charging of a large battery. **(See the section Dynamically Selectable Charge Current.)**

If the USB Dedicated Charger's current limit exceeds the CJ4054 programmed fast-charge current, then its output will regulate to 5V, and the fast-charge current will be determined by the CJ4054 PROG pin resistance to ground. If the resulting power dissipation in the CJ4054 causes an excessive rise in

temperature, then thermal limiting will reduce the charge current as needed to ensure safe charging. But if the USB Dedicated charger's current limit is less than the CJ4054 programmed fast-charge current, then its output voltage will be pulled down to the battery voltage plus charging path dropout. (The USB Dedicated Charger is required to maintain its current limit down to 2V.) This behavior is recognized in the USB Battery Charging Specification, Section 3.5, as an accepted means to reduce power dissipation in the charging circuit while charging at high current.

The CJ4054 thermal limiting and current-limited-adapter charging capability together ensure reliable charging at any programmed charge current, using any USB Battery Charging Specification compliant Dedicated Charger, regardless of its current limit.

USB and WALL ADAPTER POWER

The CJ4054 family allows charging from both a wall adapter and a USB port. Figure 18 shows an example of how to combine wall adapter and USB power inputs. A P-channel MOSFET, MP1, is used to prevent back conducting into the USB port when a wall adapter is present and a Schottky diode, D1, is used to prevent USB power loss through the 1k pull-down resistor.

Typically a wall adapter can supply more current than the 500mA-limited USB port. Therefore, an N-channel MOSFET, MN1, and an extra 10k program resistor are used to increase the charge current to 600mA when the wall adapter is present.

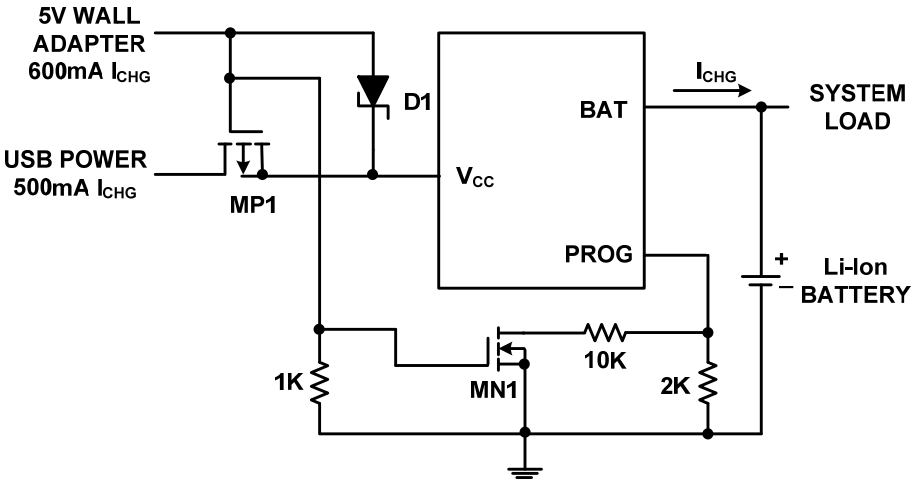


Figure 16. Combining Wall Adapter and USB Power

START UP WITH DEEPLY DEPLETED BATTERY CONNECTED

The CJ4054 charger furnishes the programmed charge current if a battery is detected. If no battery is connected, the CJ4054 operates as follows:

- The BAT pin output current is regulated to the programmed pre-charge current if $V_{BAT} < V_{TRIKL}$.
- The BAT pin output current is regulated to the programmed fast-charge current If $V_{BAT} > V_{TRIKL}$ **AND** voltage regulation is not reached.

CONNECTING THE SYSTEM LOAD TO THE BATTERY

Some designers may simply connect the system load to the battery cell. This allows the system to be powered by Li-Ion batteries without proper regulation. It is not encouraged to attach the system load directly to Li-Ion batteries when using a stand-alone Li-Ion battery charge management with automatic termination feature.

Here are several reasons that the system load is not recommended to be connected directly to the battery terminals:

1. The charge may never end. Most Li-Ion battery chargers are based on Constant Current and Constant Voltage (CC-CV) modes. The termination is based on the ratio of charge current and preset constant current (Fast Charge). If the system draws current from the battery, the charge current will never meet the termination value. This causes the non-termination of the charge management circuit.
2. The total system current is limited by the charge current because the charger will deliver total system and battery charging current through the output pin. This solution may be feasible for some applications that run on constant current, but it is not recommended.

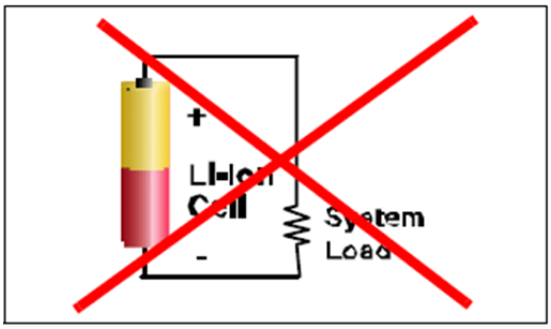
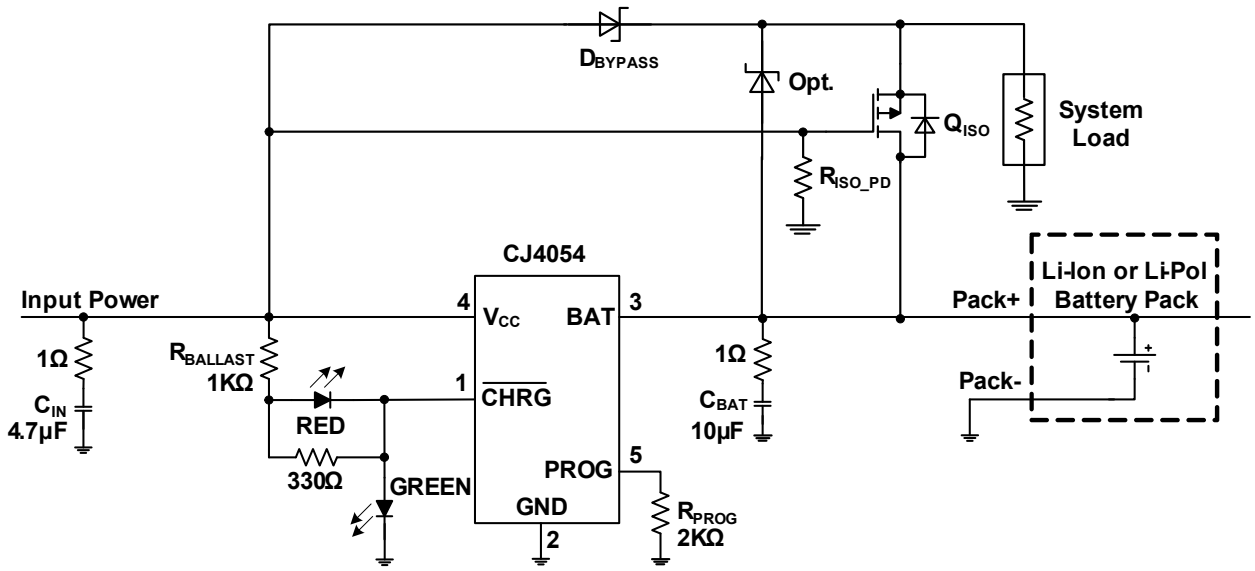


Figure 17. Do Not Connect the System Load Directly to the Battery When Charging with the Li-Ion Battery Charge Management with Automatic Termination Feature

3. A switch can be introduced to the system to turn it off before charging the batteries. This method limits the way that portable electronics operates and is only suitable for finite applications.

External Power Path Management

Some applications require that the battery be isolated from the load while charging. Figure 18 illustrates a typical charger bypass circuit. This circuit powers the load directly from the charging source via the Schottky diode D_{BYPASS}.



Typical Application for Charging Between100mA and 500mA

Figure 18. Battery Isolation and Power Path Bypass, Powering the Load Directly From the Charging Adapter

When the charging source is present, the p-channel MOSFET battery isolation switch Q_{ISO} source-to-gate voltage V_{SG} is equal to minus the D_{BYPASS} forward-biased voltage drop, ensuring that the switch Q_{ISO} is off (open). When the charging source is removed, the MOSFET gate is pulled down to ground by R_{ISO_PD}, closing the battery isolation switch and connecting the battery to the load.

When the charging source is removed, the turn-on of Q_{ISO} could be delayed due to its gate capacitance. If so, the substrate PN diode of Q_{ISO} will become forward biased, holding the load voltage to within 0.7V of the battery voltage until $V_{SG} > V_{TH}$, turning on Q_{ISO}. **This momentary voltage drop can be mitigated by the use of an optional Schottky diode in parallel with Q_{ISO}, as shown.**

With the load isolated from the battery, the charging adapter must supply both the load current and the charging current. If the sum of these should ever exceed the current capacity of the adapter, $V_{ADAPTER}$ will be pulled down. Current limited adapter operation of the CJ4054 ensures charge cycle integrity if the device load pulls the adapter voltage down to the battery voltage plus charger dropout voltage at the CC current, or even deeper into dropout if necessary to further reduce the charge current to power the device load.

Selecting The Pull-Down Resistor

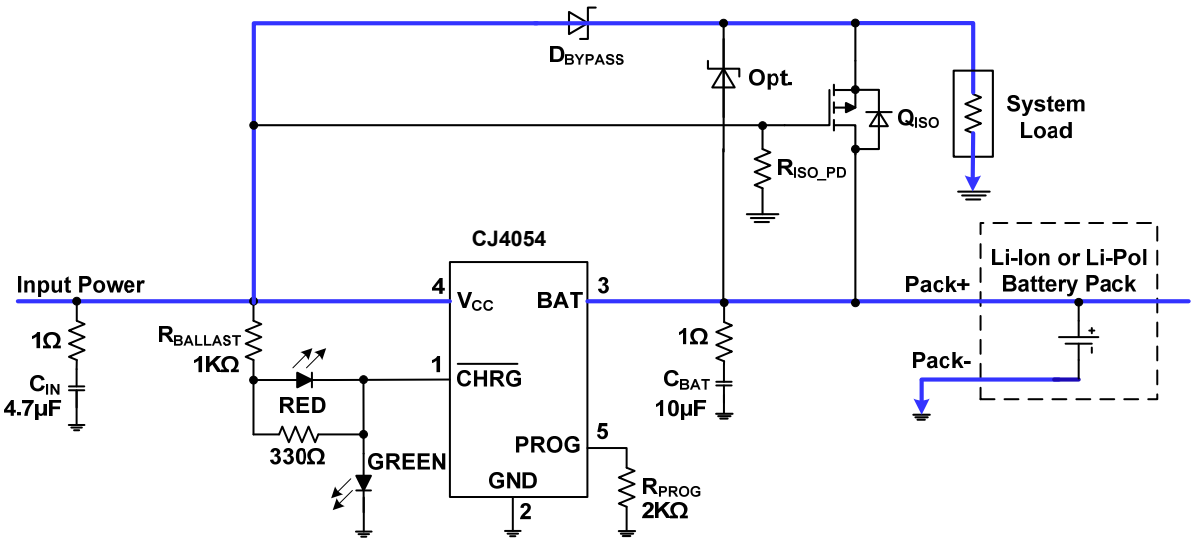
Figure 18 represents the pull-down resistor R_{ISO_PD}) to make sure that the P-Ch MOSFET (Q_{ISO}) turns on when the input sources are removed. When the input sources are absent, the R_{ISO_PD} pulls the gate to zero allowing current to flow out of the battery.

R_{ISO_PD} value can be any reasonable value resistor. However, the R_{ISO_PD} value should not be too small. A small R_{ISO_PD} value wastes unnecessary current when the input sources are present. A 100kΩ R_{ISO_PD} resistor is recommended in this design which consumes about 50μA when V_{CC}=5V.

Selecting The MOSFET

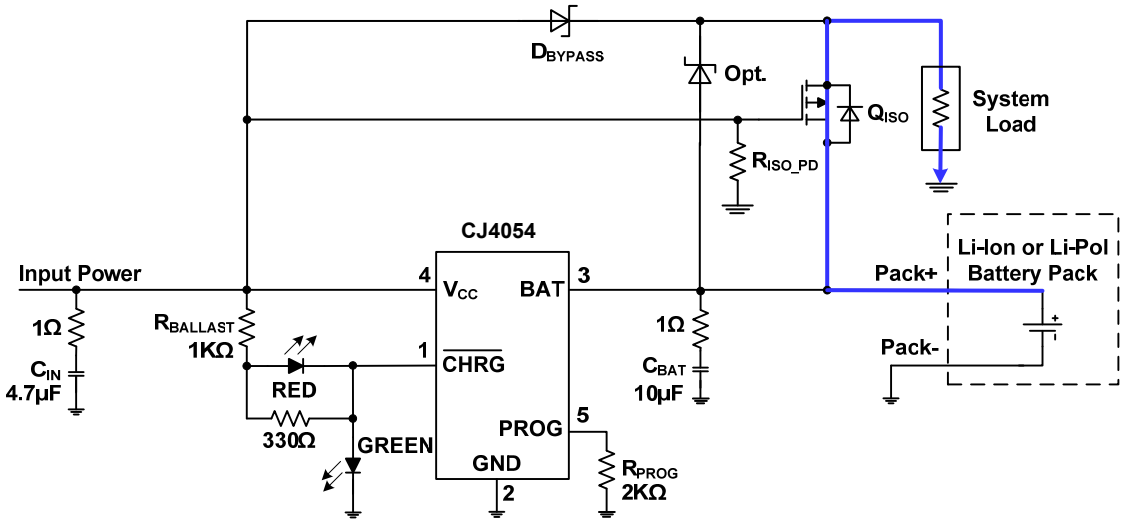
The nature of the MOSFET makes it the best candidate for current direction control. A P-Channel MOSFET is selected to complete this circuit as Figure 19 depicts, when V_{CC} is available, the gate of Q_{ISO} is high. With Q_{ISO} off, current does not flow from the Li-Ion battery to the system load. The system load requirements are provided by the input source when the Li-Ion battery is charged at the same time. When the gate of Q_{ISO} is low, Q_{ISO} turns on and allows the Li-Ion battery to supply the system as shown in Figure 20. The CJ4054 device BAT pin is also disabled when V_{CC} is absent.

Note: It is important to select a proper gate threshold voltage range so the MOSFET will be turned on.



Typical Application for Charging Between 100mA and 500mA

Figure 19. Q_{ISO} is Off When Gate is High and No Current Flows from the Battery Cell to the System Load.



Typical Application for Charging Between 100mA and 500mA

Figure 20. Q_{ISO} is On When the Gate is Low and Current Flows from the Battery Cell to the System Load.

Selecting The Diode

A diode, D_{BYPASS} in Figure 20 is required to prevent reverse current from flowing to the power source. Selecting the right diode can minimize the leakage current and the forward voltage drop from the power source to the system load. A schottky diode, which has lower forward voltage drop, is recommended.

Note: The Average Forward Current has to be rated greater than the maximum system load current for the application.

Co-packaged MOSFET + Schottky Diode

Semiconductor manufacturers provide a MOSFET and Schottky diode in one small package to save

board space and cost. A typical SO-8 packaged low forward voltage drop Schottky diode and power P-Ch MOSFET is used for demonstration in this section.

CHARGE PROFILE WITH SYSTEM LOAD

Figure 18 shows a complete system load and battery power path management circuit, which was designed for demonstration purposes in this section. The system load was set up at a constant 500mA rate. A deeply depleted 950mAh Li-Ion battery was used and charged by CJ4054 device. A fast charge current of USB_{High} was selected to charge 450mA in the Current Regulation Mode. The CJ4054 was designed to charge at a typical 450mA constant current when USB_{High} is selected and assured not to exceed the 500mA limit when a high-power USB port is available.

Note: The USB Specification clearly defines that a device may either be low-power at 100mA loads or high-power, consuming up to 500mA loads. All devices default to low-power. The transition to high-power is under software control. It is the responsibility of the software to ensure that adequate power is available before allowing devices to consume high-power. The number of “unit loads” a device can draw is an absolute maximum, not an average over time. (Designers should obtain the latest design specification and detailed information from the USB-IF, if USB peripherals are going to be implemented in a project.)

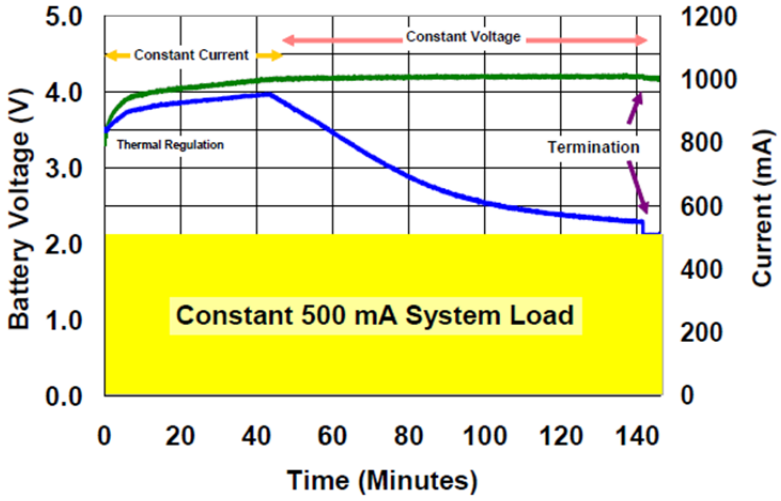


Figure 21. 450 mA Constant Charge Current Li-Ion Battery Charge Profile with a Constant 500mA System Load.

Stage 1: Preconditioning - Preconditioning is employed to restore a charge to deeply depleted cells. When the cell voltage is below the designed threshold voltage, the cell is charged with a constant current of 0.1C maximum. This period is hard to see from Figure 19 because the V_{BAT} rises above 3V in a very short period of time and enters the Current Regulation (Fast-Charge) mode.

Stage 2: Current Regulation - Once the cell voltage has risen above the preconditioning threshold, the charge current is increased to perform fast charging. The fast-charge current should not be more than 1C. A fast-charge current of 450mA (~0.5C) is used in this example. The thermal foldback period demonstrates temperature regulation by limiting the current during the Fast-Charge Period which also improve the reliability and prolongs the life of the charger IC.

Stage 3: Voltage Regulation – Fast-Charge ends and the Voltage Regulation mode is initiated when the cell voltage reaches 4.2V (4.35V option is also available for the CJ4054 for various applications). In order to maximize the capacity, the voltage regulation tolerance should be better than ±1%. The CJ4054 device provides a ±1% superior voltage regulation tolerance to deliver maximum battery run time after each completed charging cycle.

Stage 4: Termination - The CJ4054 device employs the end of charge (EOC) methods of charge current termination threshold. The CJ4054 device monitors the charge current during the constant voltage stage and terminates the charge when the charge current diminishes below approximately 0.05C (5%, 7.5%, and 20% options are available for the CJ4054 for various applications).
Note: It is not recommended to continue to trickle charge Lithium-Ion batteries.
Charging in this manner replenishes a deeply depleted battery in about 140 minutes at 0.5C. Advanced battery chargers employ additional safety features. For example, charging is suspended if the cell temperature is outside a specified window, typically 0°C to 45°C.
After 140 minutes, Figure 19 demonstrates that the power supply still supports a solid 500mA system load when charge termination occurs and the battery charger went into a charge done mode. During this charge done mode, the CJ4054 device continues to monitor the BAT pin voltage and will recharge the Li-Ion battery, once the regulated BAT pin voltage drops below 150 mV.

DISCHARGE THE LI-ION BATTERY

When a full charge cycle was completed, the input power source was removed. The P-Ch MOSFET was turned on to supply the system load with 0.53C and discharged the 950mA Li-Ion battery as shown in Figure 22. The termination duration is load dependent and Figure 25 also shows the Li-Ion battery was not able to deliver 500mA after 105 minutes. With approximately 0.5C discharge rate, the time should last about 2 hours. The main reason that the remaining 15 minutes are not available from this experiment is because the remaining capacity level is not enough to support 500mA.
Note: When fully depleted, a Li-Ion battery may degrade its life cycle and should be avoided.

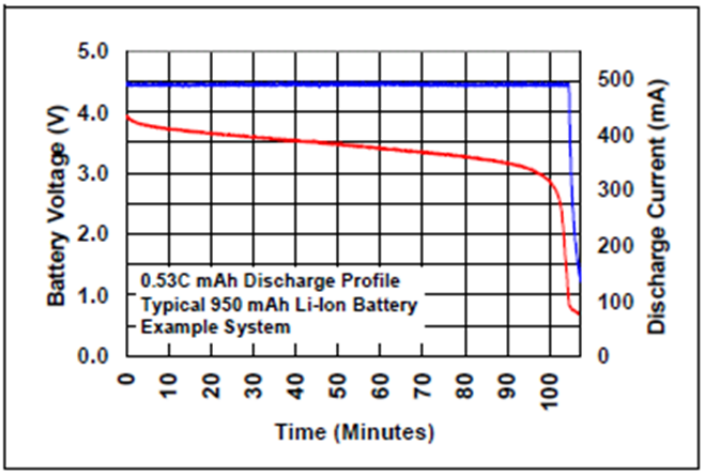


Figure 22. 500mA Discharge Profile When V_{CC} is Removed.

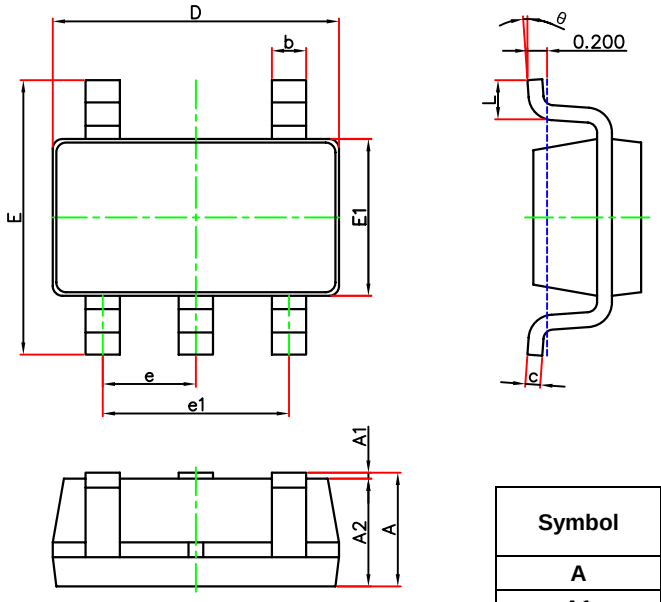
System and battery load sharing power path management circuits are very common in portable applications. Adapting this simple design wisely can dramatically reduce the total system cost and product developing time in order to take advantages of using a fully integrated battery charge management.

■ PCB LAYOUT CONSIDERATIONS

The CJ4054 series are fully integrated single-chip low cost single-cell Li-Ion or Li-Pol battery chargers ideal for portable applications. Careful PCB layout is necessary. For optimal performance, place all peripheral components as close to the IC as possible. A short connection is highly recommended. Several layout tips are listed below for the best electric and thermal performance.

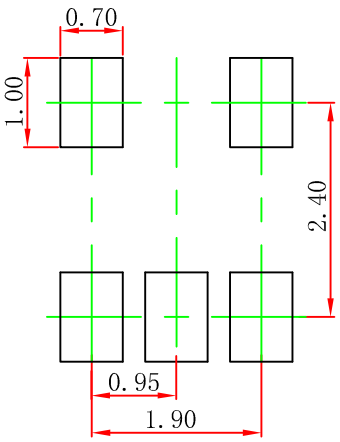
- Input bypass capacitor from V_{CC} to GND should be placed as close as possible to CJ4054, with short trace runs to both V_{CC} and GND pins, and connected to ground plane. The trace of input in the PCB should be placed far away the sensitive devices or shielded by the ground.
- The GND should be connected to a strong ground plane for heat sinking and noise protection.
- Output bypass capacitors from BAT to GND should be placed as close as possible to CJ4054, with short trace runs to both BAT and GND pins, and connected to ground plane to reduce noise coupling.
- The connection of R_{PROG} should be isolated from other noisy traces. The short wire is recommended to prevent EMI and noise coupling.
- All low-current GND connections should be kept separate from the high-current charge or discharge paths from the battery. Use a single-point ground technique incorporating both the small signal ground path and the power ground path.
- The BAT pin is the voltage feedback to the device and should be connected with its trace as close to the battery pack as possible.
- The high current charge paths into V_{CC} pin and from the BAT pin must be sized appropriately for the maximum charge current in order to avoid voltage drops in these traces.

SOT-23-5L Package Outline Dimensions



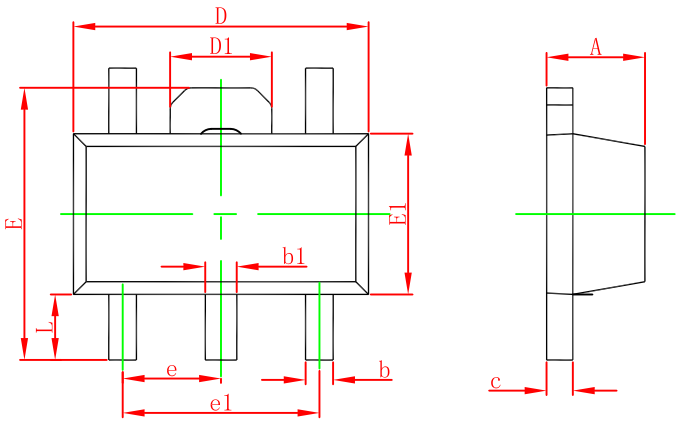
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	2.650	2.950	0.104	0.116
E1	1.500	1.700	0.059	0.067
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

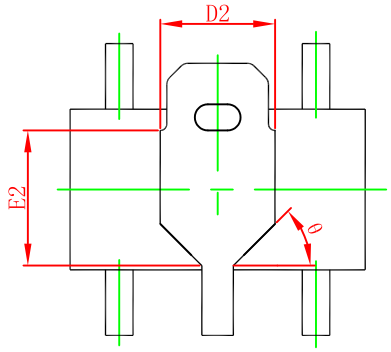
SOT-23-5L Suggested Pad Layout



Note:
1.Controlling dimension:in millimeters.
2.General tolerance:±0.05mm.
3.The pad layout is for reference purposes only.

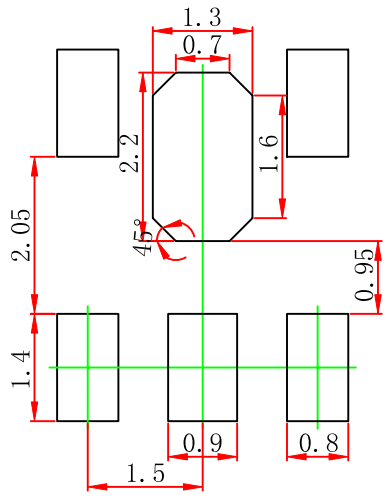
SOT-89-5L Package Outline Dimensions





Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.400	1.600	0.055	0.063
b	0.320	0.520	0.013	0.020
b1	0.360	0.560	0.014	0.022
c	0.350	0.440	0.014	0.017
D	4.400	4.600	0.173	0.181
D1	1.400	1.800	0.055	0.071
E	2.300	2.600	0.091	0.102
E1	3.940	4.250	0.155	0.167
e	1.500TYP		0.060TYP	
e1	2.900	3.100	0.114	0.122
L	0.900	1.100	0.035	0.043

SOT-89-5L Suggested Pad Layout



Note:
1.Controlling dimension:in millimeters.
2.General tolerance:±0.05mm.
3.The pad layout is for reference purposes only.

DISCLAIMER

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