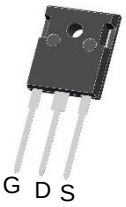
CJWT030JN65AD

CJWT030JN65AD

Parameter	Value	Unit
$V_{DS}@T_{J, MAX}$	650	V
$R_{DS(on)TYP}$	26	mΩ
$Q_{g, typ}$	226	nC
I_D	80	A

TO-247



DESCRIPTION

This device used high Voltage of advanced balanced junction technology, has extremely low $R_{DS(ON)}$ and Gate charge, it fits in applications which require superior power density and outstanding efficiency.

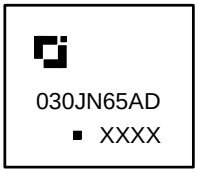
FEATURE

- 600V Breakdown Voltage
- Ultra Low $R_{DS(ON)}$ =30mΩ@V_{GS} =10V
- New Technology in High Voltage Device
- Ultra Low Gate Charge
- 100% Avalanche Tested

APPLICATIONS

- EV Charger
- Power Factor Correction (PFC)
- Solar Power
- Power Storage

MARKING

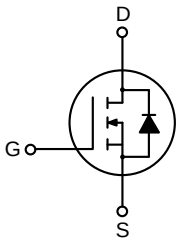


030JN65AD =Device code.

Solid dot =Green molding compound device, if none, the normal device

XXXX =Code

EQUIVALENT CIRCUIT



Order Code	Package	Marking	Parking
CJWT030JN65AD	TO-247	030JN65AD	Tube

Absolute Maximum Ratings (T_C=25°C unless otherwise noted)

Symbol	Parameter	Value	Unit
V_{DSS}	Drain-Source Voltage	600	V
V_{GSS}	Gate-Source Voltage	±20	V
	Gate-Source transient voltage, AC (f >1Hz)	±30	
I_D	Drain Current	80	A
	Drain Current @T_C=100℃	50	
I_{DM}	Pulsed Drain Current, tp limited by $T_{J, MAX}$	240	A
E_{AS}	Avalanche Energy, Single Pulse (1)	2500	mJ
I_S	Continuous Diode Forward Current	80	A
$I_{S. PULSE}$	Diode Pulsed Current, limited by $T_{J, MAX}$	240	A
dv/dt	MOSFET dv/dt Ruggedness, V_{DS}≤480V	50	V/nS
	Reverse Diode dv/dt, V_{DS}≤480V, I_{SD}≤I_D	50	
P_D	Power Dissipation @T_C=25℃	481	W
T_J, T_{STG}	Junction and Storage Temperature Range	-55 to 150	℃

(1) V_{DD} = 100V, R_G = 25Ω, L=60mH, Starting T_J = 25°C.

Thermal Characteristics

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal resistance, Maximum Junction-to-Case	0.26	℃/W
$R_{\theta JA}$	Thermal resistance, Maximum Junction-to-Ambient	62	℃/W

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Ration			Unit
			Min.	Typ.	Max.	
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250uA	600			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{GS}=0V, V_{DS}=600V			100	μA
I_{GSS}	Gate-Source leakage current	V_{GS}=±20V			±200	nA
		V_{GS}=±30V			±500	nA
$V_{GS(th)}$	Gate-Source Threshold Voltage	I_D=2.2mA, V_{DS}=V_{GS}	3		5	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	I_D=35A, V_{GS}=10V		26	30	mΩ
V_{SD}	Drain-Source Diode Forward Voltage	I_{SD}=35A, Tc =25℃			1.5	V
DYNAMIC PARAMETERS						
C_{ISS}	Input Capacitance	V_{DS}=50V, V_{GS}=0V f =100KHz		8473		pF
C_{OSS}	Output Capacitance			457		
C_{RSS}	Reverse Transfer Capacitance			13		
$C_{O(er)}$	Effective output capacitance, energy Related (2)	V_{GS}=0V, V_{DS}=0…400V		300		pF
$C_{O(tr)}$	Effective output capacitance, time Related (3)			1850		pF
Rg	Gate resistance	Open Drain, f =1MHz		2.4		Ω
SWITCHING PARAMETERS						
$t_{d(on)}$	Turn-On Delay Time	V_{DD}=400V, I_D=40A R_G=2Ω, V_{GS}=10V, T_J=25°C		39		ns
t_r	Current Rise Time			40		
$t_{d(off)}$	Turn-Off Delay Time			148.8		
t_f	Current Fall Time			4.2		
Gate Charge Characteristics						
Q_{gs}	Gate to source charge	V_{DD}=400V, I_D=40A V_{GS}=0 to 10V		56.7		nC
Q_{gd}	Gate to drain charge			115.1		
Q_g	Gate charge total			226.2		
Reverse Diode Characteristics						
t_{rr}	Reverse recovery time	V_R=400V, I_F=30A dI_F/dt =100A/us		175		nS
Q_{rr}	Reverse recovery charge			1.3		μC
I_{rrm}	Peak reverse recovery current			13.9		A

（2）$C_{O(er)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 400V.

（3）$C_{O(tr)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 400V.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

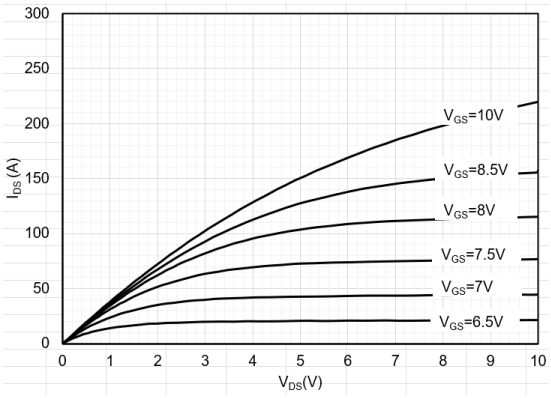


Figure 1: Output Characteristic

(T_J=25°C)

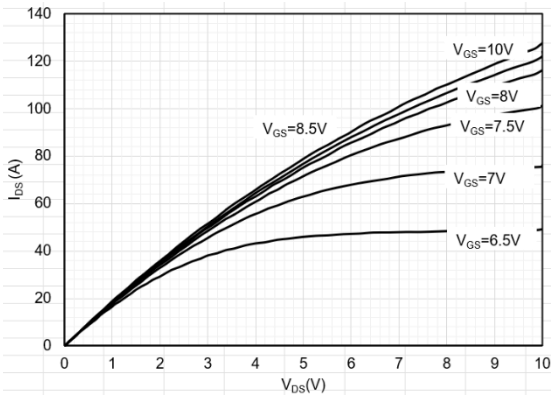


Figure 2: Output Characteristic

(T_J=125°C)

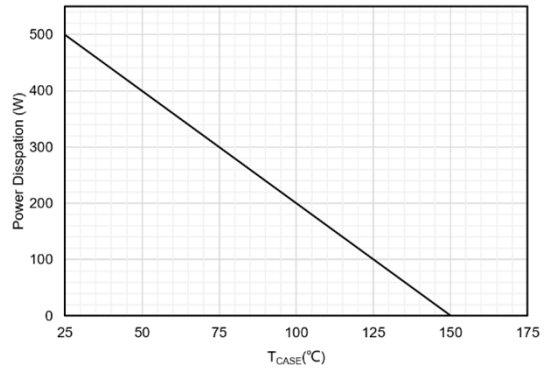


Figure 3: Power Dissipation

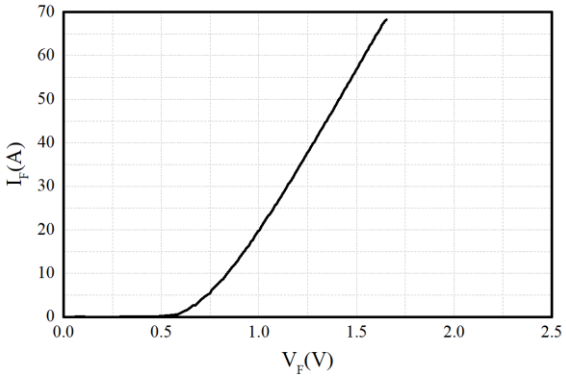


Figure 4: Diodе Characteristic

(T_J=25°C)

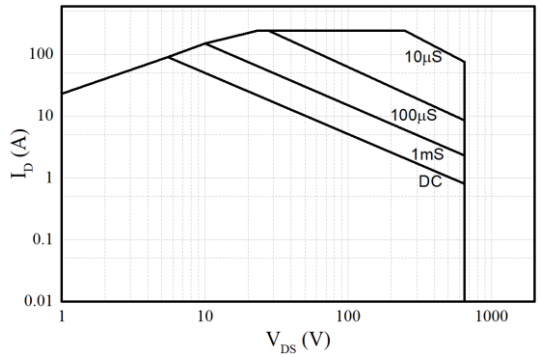


Figure 5: Safe Operating Area

(T_C=25°C, V_{GS}≥8V)

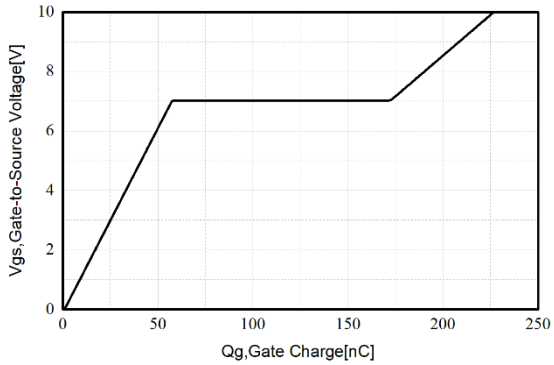


Figure 6: Typ. Gate charge

(V_D=400V, I_D=40A)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

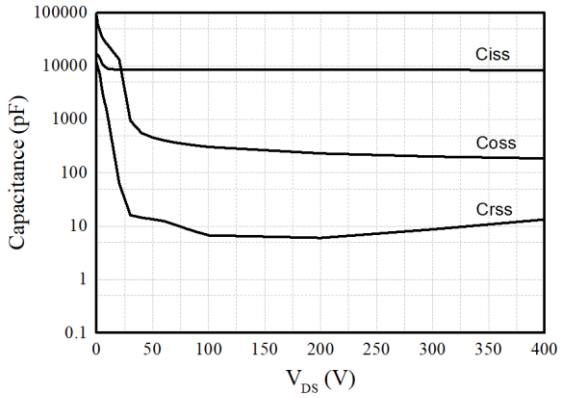


Figure 7: Typ. Capacitances

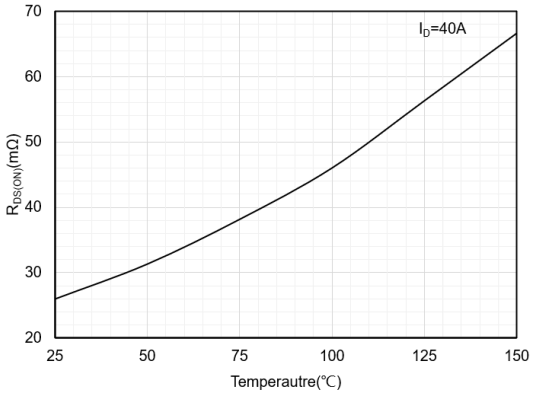


Figure 8: Drain-source on-state resistance

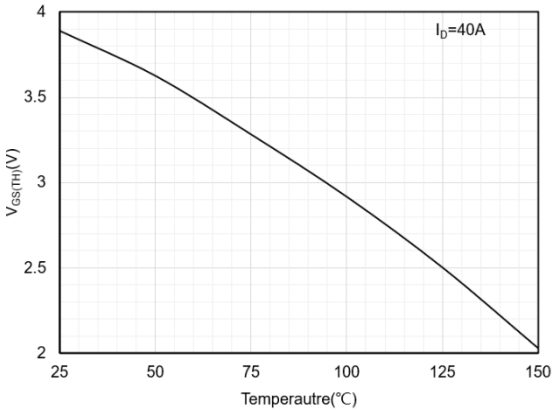


Figure 9: Threshold voltage

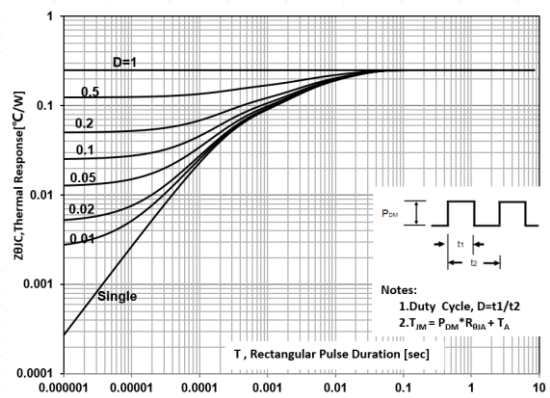


Figure 10: Max. transient thermal impedance

TEST CIRCUIT AND WAVEFORMS

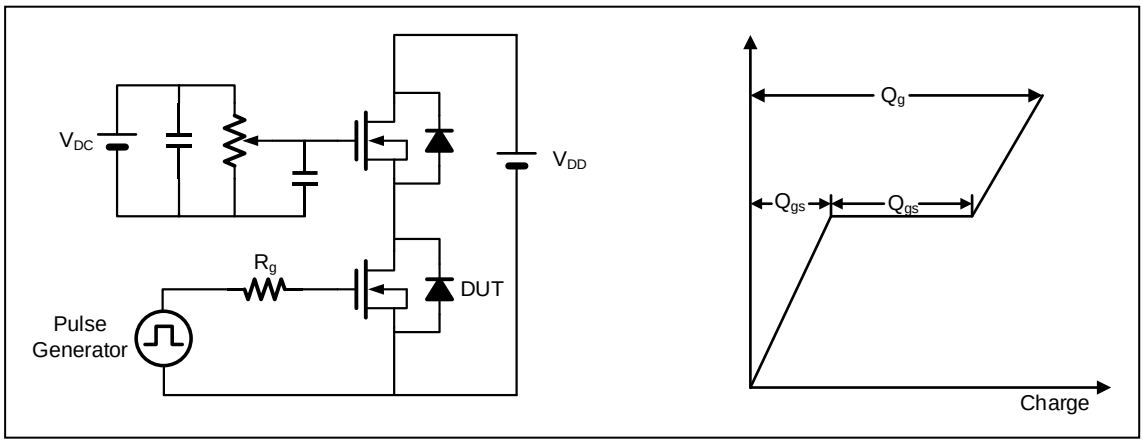


Figure 1: Gate Charge test circuit & waveform

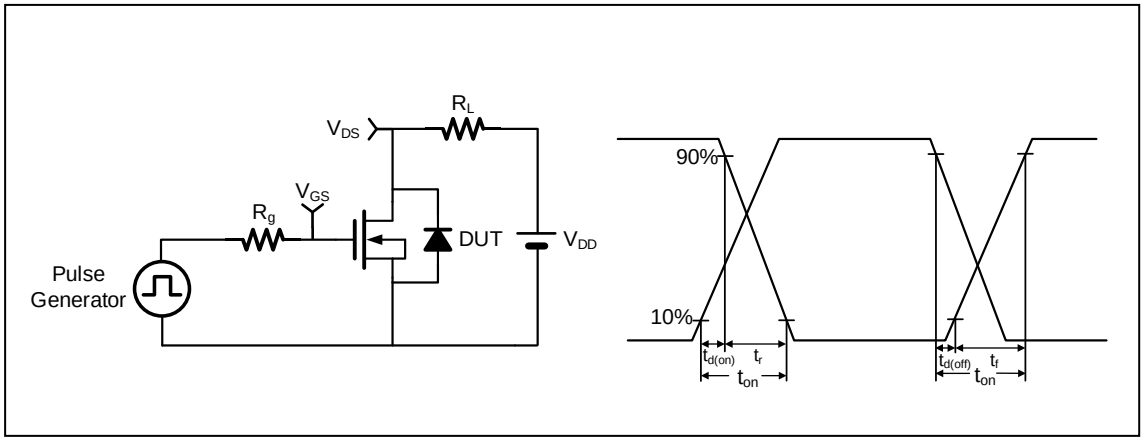


Figure 2: Resistive load switching time test circuit & waveforms

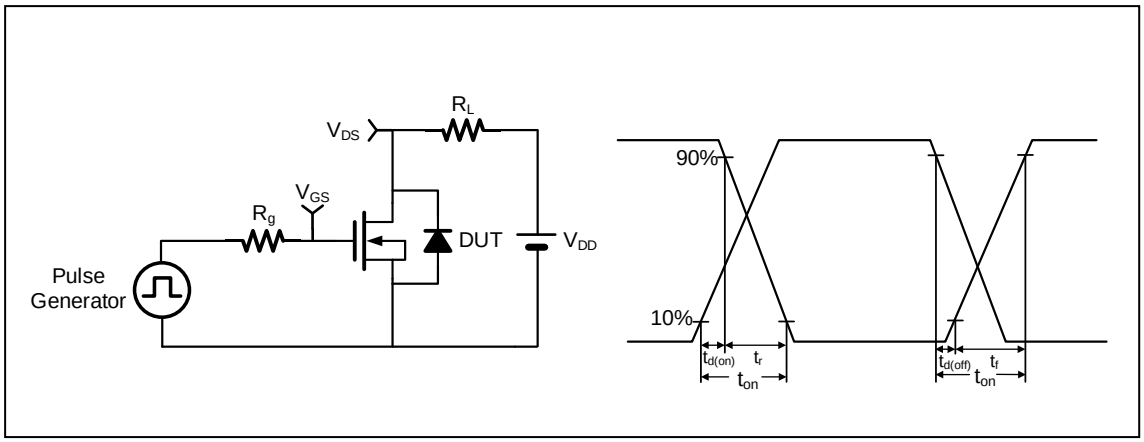
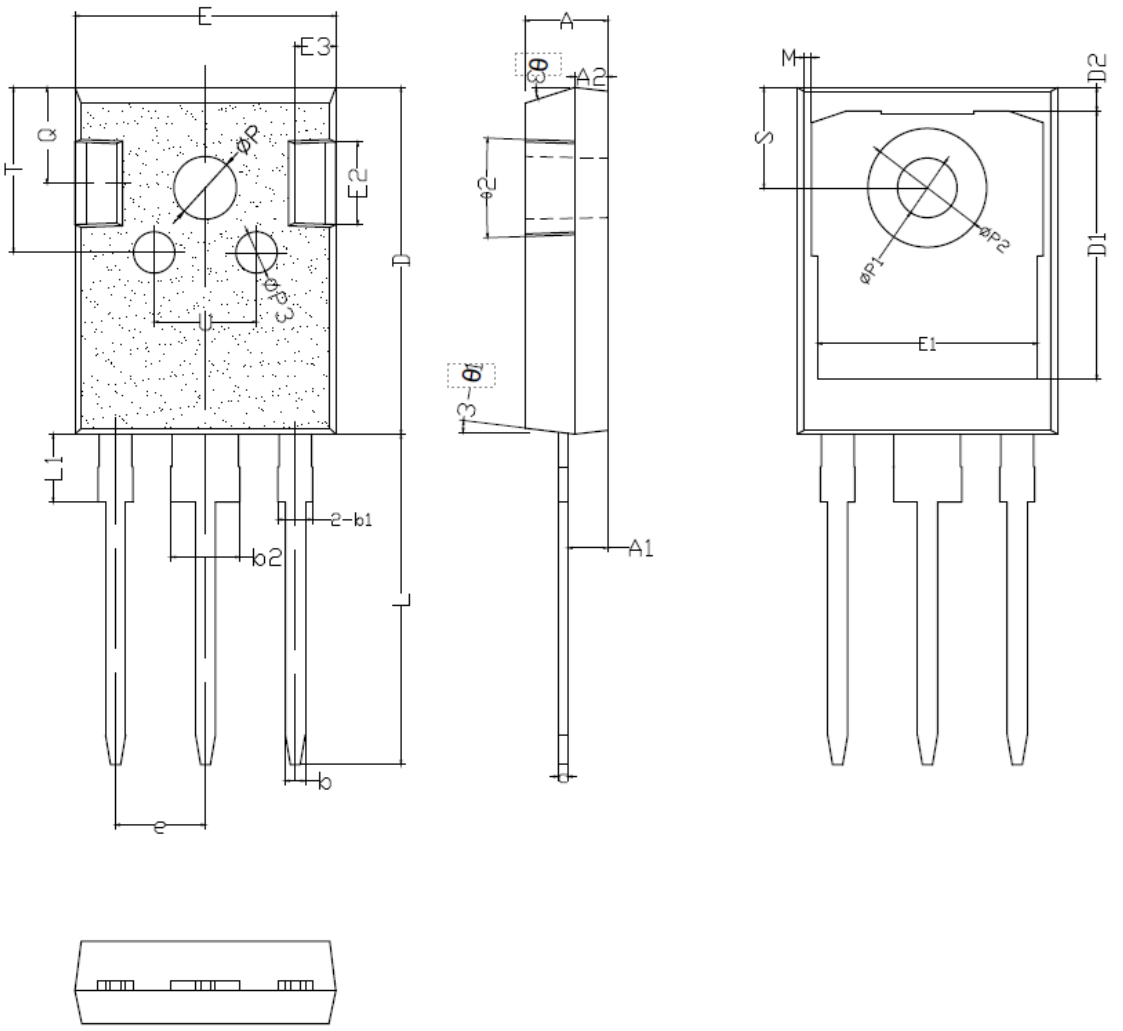


Figure 3: Un-clamped inductive switching (UIS) test circuit & waveforms

TO-247 PACKAGE OUTLINE DIMENSIONS



SYMBOL	mm		
	MIN	NOM	MAX
*A	4.90	5.00	5.10
*A1	2.31	2.41	2.51
A2	1.90	2.00	2.10
*b	1.15	1.20	1.25
*b1	1.95	2.10	2.25
*b2	2.95	3.10	3.25
*c	0.55	0.60	0.65
*D	20.90	21.00	21.10
D1	16.35	16.55	16.75
D2	1.05	1.20	1.35

*E	15.70	15.80	15.90
E1	13.10	13.25	13.40
E2	4.85	4.95	5.10
E3	2.40	2.50	2.60
*e	5.40	5.44	5.48
*L	19.80	19.98	20.15
*L1	-	-	4.30
*ΦP	3.40	3.50	3.60
*ΦP1	6.90	7.10	7.30
ΦP2	2.40	2.50	2.60
ΦP3	2.40	2.50	2.60
Q	5.60	5.80	6.00
*S	6.05	6.15	6.25
T	9.80	10.00	10.20
U	6.00	6.20	6.40
θ1	5°	7°	9°
θ2	1°	3°	5°
θ3	13°	15°	17°
*为管控尺寸			