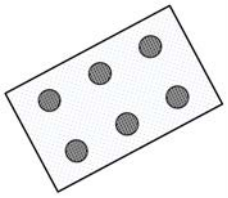
SZCJ Shenzhen Changji Semiconductor Co., LTD.

CSP Enhancement Mode Power MOSFET

CJ13024SP Dual N-Channel MOSFET

V_{SSS}	$R_{SS(on)}$TYP	I_S
12V	4.7mΩ@4.5V	9A
	5.0mΩ@3.8V	
	5.5mΩ@3.1V	
	6.5mΩ@2.5V	

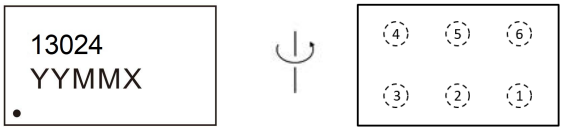
CSPB1912-6



DESCRIPTION

The CJ13024SP uses advanced trench technology to provide excellent $R_{SS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V while retaining a 8V $V_{GS(MAX)}$ rating. It is ESD protected. This device is suitable for use as a unidirectional or bi-directional load switch, facilitated by its common-drain configuration.

Marking and pin assignment



Topside view Bottom View

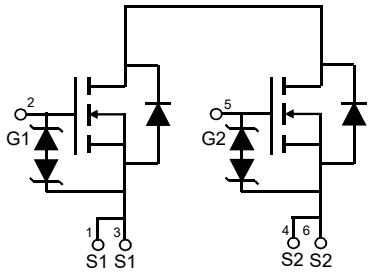
Marking:

1. 13024: Product Code
2. YYMMX: Date Code
3. Solid dot: Pin 1

1,3. Source1 2. Gate1

4,6. Source2 5. Gate2

Equivalent Circuit



ABSOLUTE MAXIMUM RATINGS (T_J=25℃ unless otherwise noted)

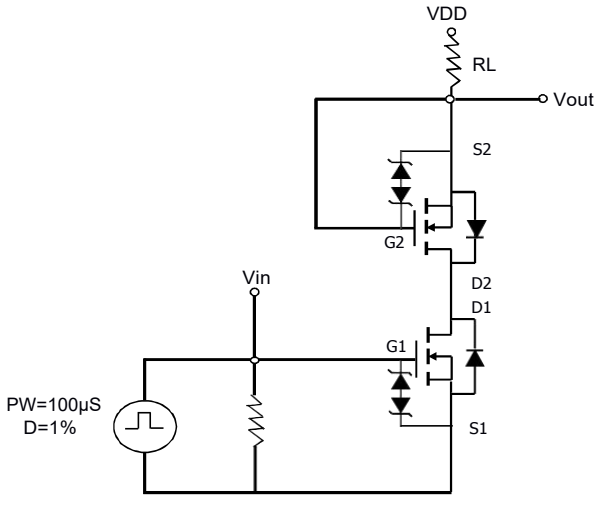
Parameter	Symbol	Limit	Unit
Source to Source Voltage	V_{SSS}	12	V
Gate-Source Voltage	V_{GSS}	±8	V
Source Current(DC)	I_S ①	9	A
Source Current(DC)	I_S ②	15	A
Source Current (Pulsed)	I_{SP} ③	90	A
Total Power Dissipation	P_T ①	2.1	W
Channel Temperature	T_{ch}	150	℃
Storage Temperature Range	T_{STG}	-55 To 150	℃

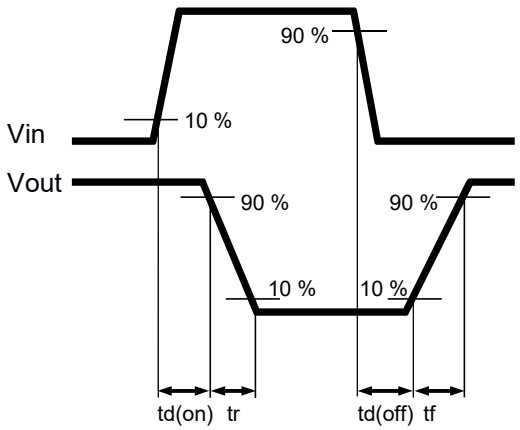
MOSFET ELECTRICAL CHARACTERISTICS

T_J=25 ℃ unless otherwise specified

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static Parameters						
Source to Source Breakdown Voltage	BV_{SSS}	I_S=1mA ,V_{GS}=0V	12			V
Zero-Gate Voltage Source Current	I_{SSS}	V_{SS}=10V,V_{GS}=0V			100	nA
Gate to Source Leakage Current	I_{GSS}	V_{SS}=0V, V_{GS}= ±8V			±10	μA
Gate to Source Threshold Voltage	$V_{GS(th)}$	V_{SS}=V_{GS}, I_S=0.26mA	0.4	0.8	1.4	V
Source to Source On-state Resistance	$R_{SS(on)}$	V_{GS}=4.5V,I_S=2A	3.0	4.7	5.4	mΩ
		V_{GS}=3.8V,I_S=2A	3.3	5.0	6.0	mΩ
		V_{GS}=3.1V,I_S=2A	3.5	5.5	7.7	mΩ
		V_{GS}=2.5V,I_S=2A	4.5	6.5	13.6	mΩ
Input Capacitance	Ciss	V_{SS}=6V, V_{GS}=0V,f=100kHZ		1417		pF
Output Capacitance	Coss			463		pF
Reverse Transfer Capacitance	Crss			360		pF
Turn-on Delay Time	$t_{d(on)}$ ④	V_{DD}=6V,R_L=1.3Ω V_{GS}=4V		269		nS
Turn-on Rise Time	t_r ④			329		nS
Turn-off Delay Time	$t_{d(off)}$ ④			1377		nS
Turn-off Fall Time	t_f ④			1253		nS
Total Gate Charge	Q_g ④	V_{SS}=10V,I_S=10A,V_{GS}=6V		37.8		nC
Gate1-source1 charge	Q_{g1s1} ④			2.4		nC
Gate1-source2 charge	Q_{g1s2} ④			7.7		nC
Diode Forward Voltage	$V_{F(S-S)}$	V_{GS}=0V,I_S=2A			1.2	V

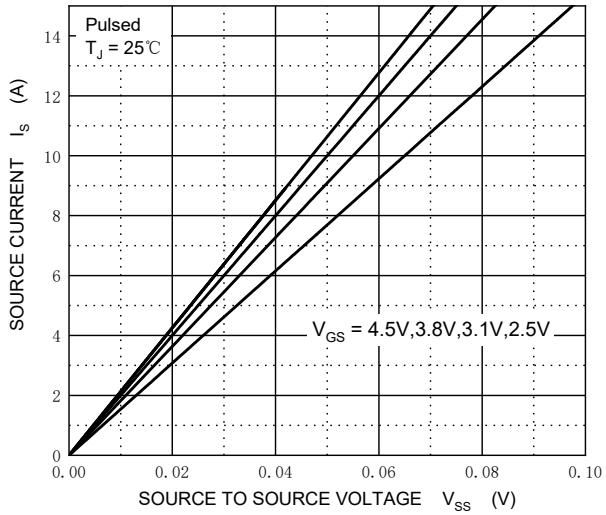
Notes: 1.Mounted on FR4 board (25.4mm×25.4mm×t1.0mm) using minimum recommended pad size (partial coverage of single-sided 36um Copper).
2. Mounted on FR4 board(25.4mm×25.4mm×t1.0mm) using minimum recommended pad size (full coverage of single-sided 36um Copper).
3. t = 10 μs , Duty Cycle ≤ 1 %.
4. When FET1 is measured,G2 and S2 are short-circuited.



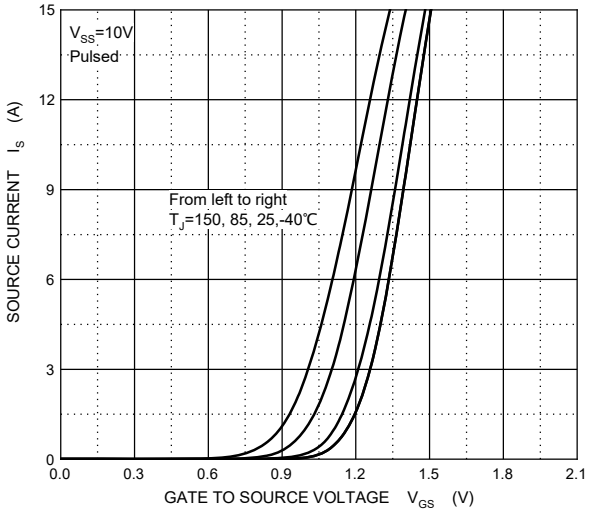


Typical Characteristics

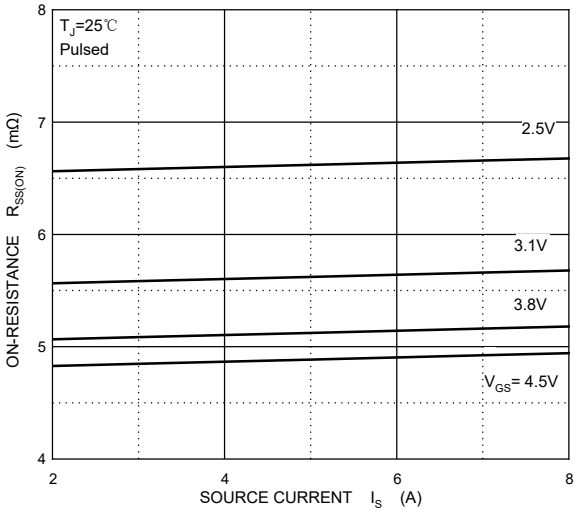
I_S—V_{SS}



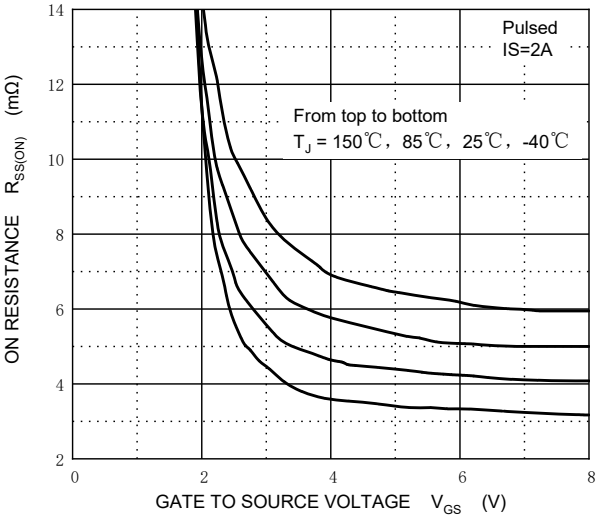
IS-VGS



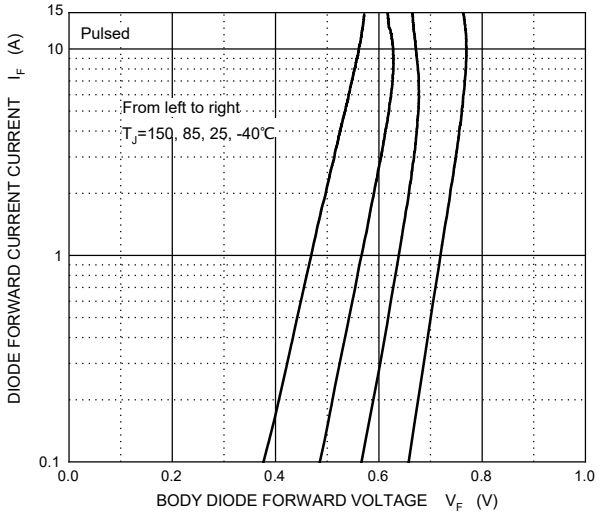
$R_{SS(ON)}$ —— I_S



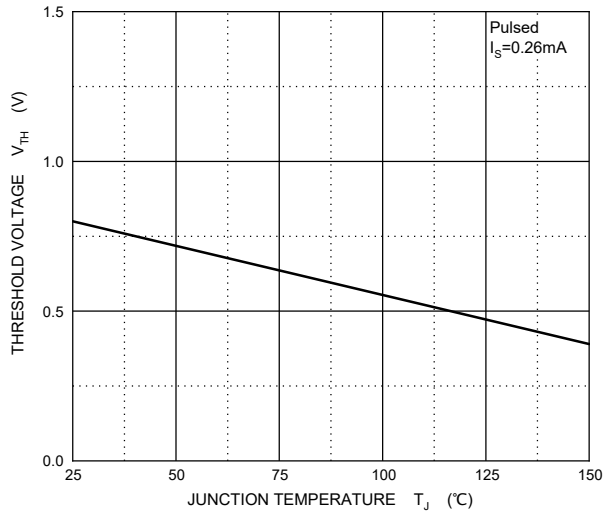
$R_{ss(on)}$—V_{GS}



I_F —— V_F

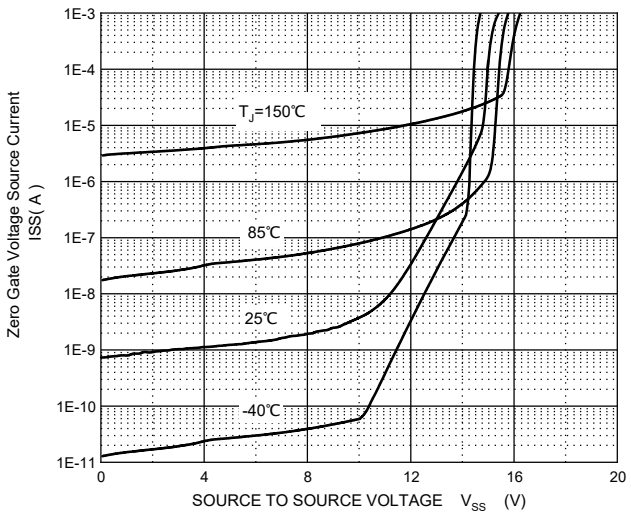


Threshold Voltage

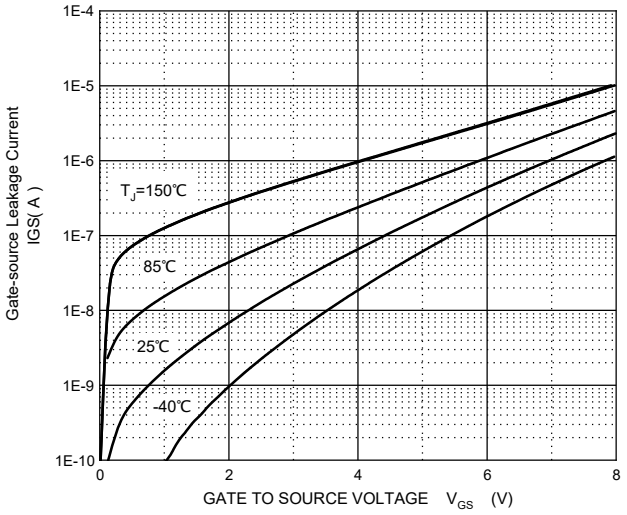


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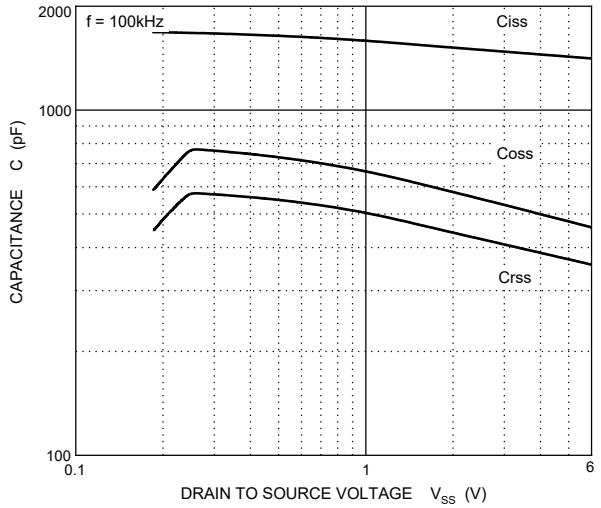
ISS-VSS



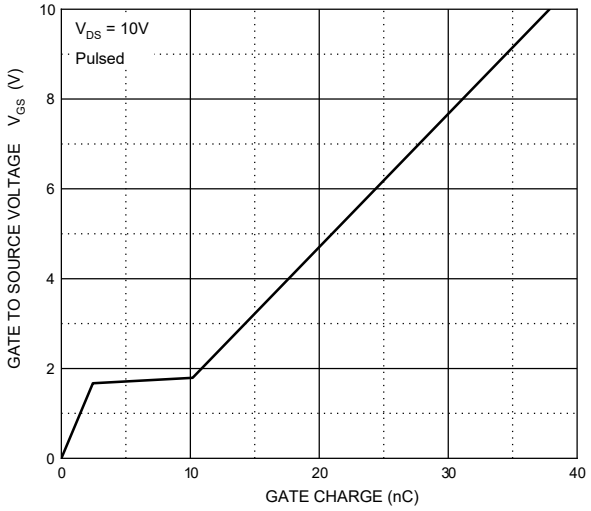
IGS-VGS



Typical Capacitances

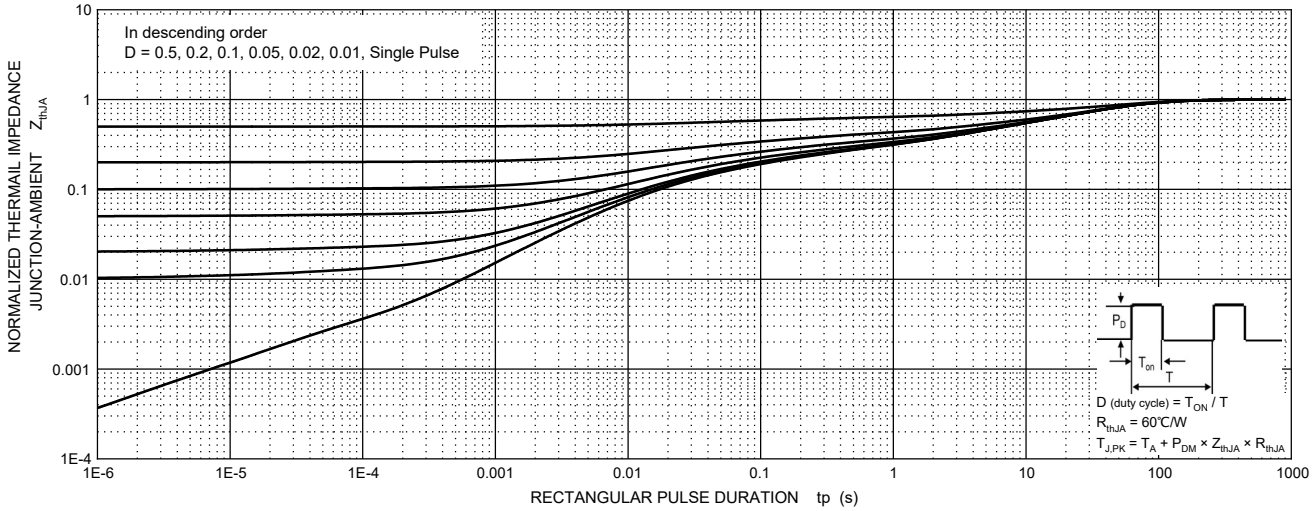


Gate Charge

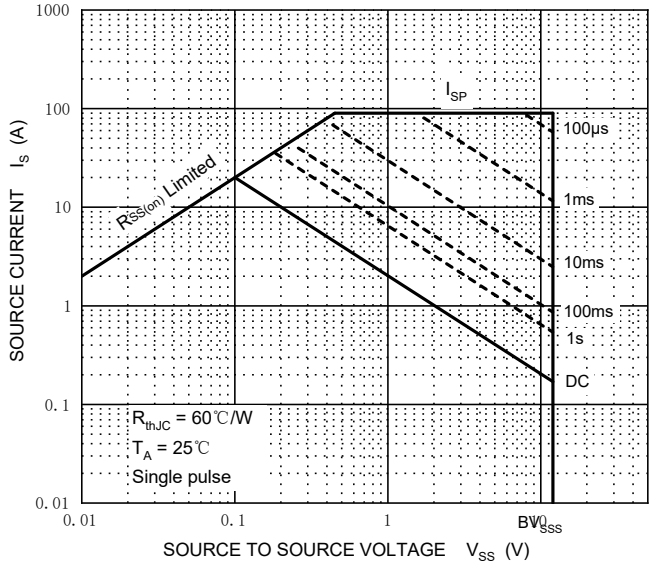


Typical Characteristics

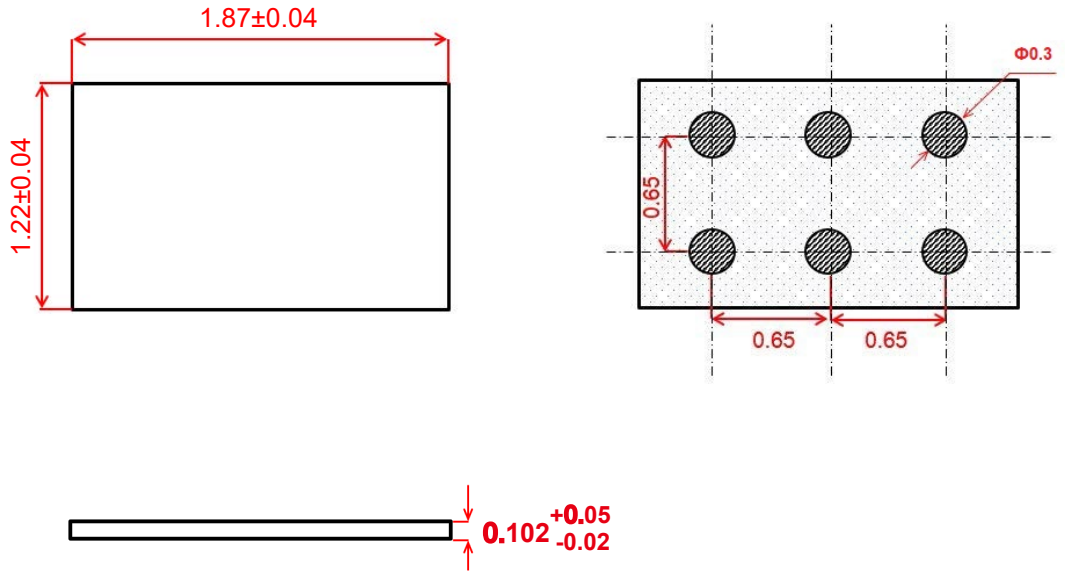
Transient Thermal Impedance, Junction-Ambient



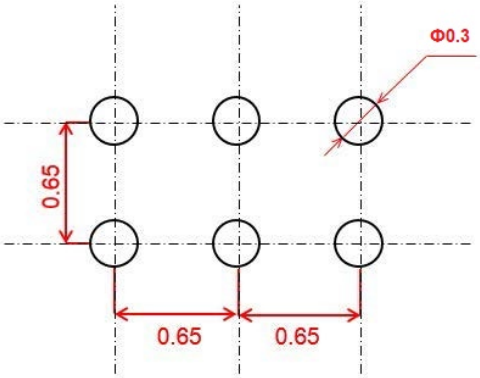
Maximum Safe Operating Area



CSPB1912-6 Package Outline Dimensions(Unit:mm)



CSPB1912-6 Suggested Pad Layout (Unit:mm)



Note:
1.Controlling dimension:in millimeters.
2.General tolerance:± 0.050mm.
3.The pad layout is for reference purposes only.

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