Zero-Drift, Micro-Power, 1.5 MHz, RRIO Operational Amplifiers

CJOA855x Series Operational Amplifiers

1 Introduction

The CJOA855x family of amplifiers provides input offset voltage correction for very low offset and drift through the use of patented fast step response chopper stabilized techniques. This method constantly measures and compensates the input offset, eliminating drift over time and temperature and the effect of 1/f noise. This design breakthrough allows the combination of a gain bandwidth product of 1.5MHz and a high slew rate of 1.2V/μs, while only drawing 125μA supply current. These devices are unity gain stable and have good Power Supply Rejection Ratio (PSRR) and Common Mode Rejection Ratio (CMRR).

The CJOA855x series are perfectly suited for applications that require precision amplification of low level signals, in which error sources cannot be tolerated, even in which high bandwidth and fast transition are needed. The rail-to-rail input and output swings make both high-side and low-side sensing easy. The CJOA855x series can operate with a single supply voltage as low as 1.8V for 2-cell battery applications.

The CJOA855x op-amps have enhanced EMI protection to minimize any electromagnetic interference from external sources, and have high electro-static discharge (ESD) protection (5kV HBM). All models are specified over the extended industrial temperature range of -40°C to +125°C.

2 Features

- High DC Precision:
  ±8μV (Max.) V_{OS} with a Drift of ±40nV/°C (Max.)
  A_{VOL}: 112dB (Min.)
  PSRR: 112dB (Min.)
  CMRR: 112dB (Min.)
  V_n: 0.45μV_{PP} (typical, f = 0.1 to 10Hz)
- 1.5MHz Bandwidth and 1.2V/μs Slew Rate
- Settling Time to 0.1% with 1V Step: 1.2μs
- Overload Recovery Time to 0.1%: 35μs
- Micro-Power 125μA per Amplifier and 1.8V to 5.5V Wide Supply Voltage Range
- Operating Temperature Range:
  −40°C to +125°C

3 Applications

- Precision current sensing
- Resistor thermal detectors
- Temperature, position and pressure sensors
- Medical equipment
- Electronic scales
- Strain gage amplifiers
- Thermocouple amplifiers
- Driving A/D Converters

4 Available Packages

PART NUMBER	PACKAGE
CJOA8551-M5N	SOT-23-5L
CJOA8552-PAN	SOP8
CJOA8552-PDN	MSOP8
CJOA8552-DCN	DFNWB2×2-8L

5 Orderable Information

MODEL	DEVICE	PACKAGE	OP TEMP	ECO PLAN	MSL	PACKING OPTION	SORT
CJOA8551	CJOA8551-M5N	SOT-23-5L	-40 ~ 125°C	RoHS & Green	Level 3 168 HR	Tape and Reel 3000 Units / Reel	Active
CJOA8552	CJOA8552-PAN	SOP8	-40 ~ 125°C	RoHS & Green	Level 3 168 HR	Tape and Reel 4000 Units / Reel	Active
	CJOA8552-PDN	MSOP8	-40 ~ 125°C	RoHS & Green	Level 3 168 HR	Tape and Reel 4000 Units / Reel	Active
	CJOA8552-DCN	DFNWB2×2-8L	-40 ~ 125°C	RoHS & Green	Level 3 168 HR	Tape and Reel 3000 Units / Reel	Active
Others	-	-	-	-	-	-	Customized

Note:

ECO PLAN: For the RoHS and Green certification standards of this product, please refer to the official report provided by SZCJ .

MSL: Moisture Sensitivity Level. Determined according to JEDEC industry standard classification.

SORT: Specifically defined as follows:

Active: Recommended for new products;

Customized: Products manufactured to meet the specific needs of customers;

Preview: The device has been released and has not been fully mass produced. The sample may or may not be available;

NoRD: It is not recommended to use the device for new design. The device is only produced for the needs of existing customers; Obsolete: The device has been discontinued.

6 Pin Configuration and Marking Information

6.1 Pin Configuration and Function

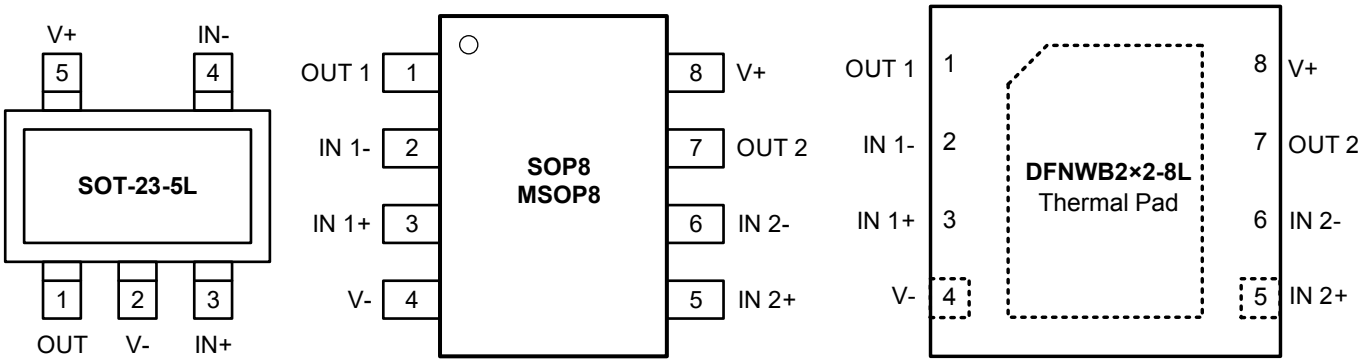
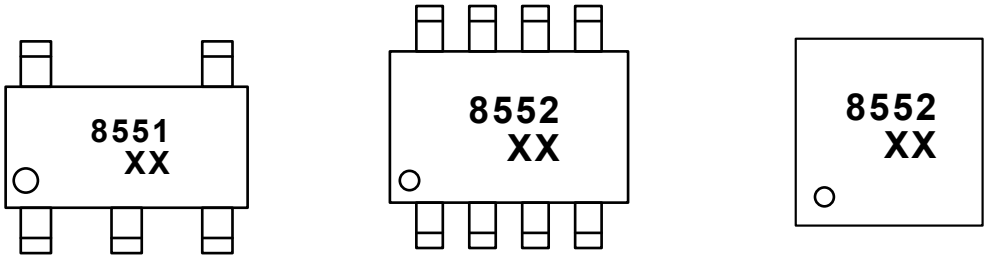


Figure 6-1. CJOA855x Pin Map

PIN NAME	CJOA8551 SOT-23-5L	CJOA8552 SOP8/MSOP8/DFNWB2×2-8L	I / O	DESCRIPTION
OUT 1	1	1	O	Output of the operational amplifier 1.
IN 1-	4	2	I	Negative input of the operational amplifier 1.
IN 1+	3	3	I	Positive input of the operational amplifier 1.
V+	5	8	-	Positive (highest) supply.
IN 2+	-	5	I	Positive input of the operational amplifier 2.
IN 2-	-	6	I	Negative input of the operational amplifier 2.
OUT 2	-	7	O	Output of the operational amplifier 2.
V-	2	4	-	Negative (lowest) supply or ground for single supply.

6.2 Marking Information



SOT-23-5L **SOP8/MSOP8** **DFNWB2×2-8L**

"**855x**": Device number.

"**XX**": Code, indicates weekly record information.

7 Specifications

7.1 Absolute Maximum Ratings

(over operating ambient temperature range, unless otherwise specified)(1)

CHARACTERISTIC		SYMBOL	VALUE	UNIT
Supply voltage[(V+) - (V-)]		V_S	10	V
Signal input pins	Voltage(2)		(V-)-0.5V ~ (V+)+0.5V	V
	Current(2)		±20	mA
Output short-circuit		T_{sc}	Continuous(3)	mA
Maximum junction temperature		$T_{J\ MAX}$	150	°C
Storage temperature		T_{stg}	-65 ~ 150	°C
Soldering temperature & time		T_{solder}	260°C, 10s	-

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum rated conditions for extended periods may affect device reliability.

(2) Input pins are diode-clamped to the power-supply rails. Current limit input signals that can swing more than 0.5V beyond the supply rails to 10mA or less.

(3) Short circuits from outputs to V_S can cause excessive heating and eventual destruction. A heat sink may be required to keep the junction temperature below the absolute maximum. This depends on the power supply voltage and how many amplifiers are shorted. Thermal resistance varies with the amount of PC board metal connected to the package. The specified values are for short traces connected to the leads.

7.2 Recommend Operating Conditions

(over operating ambient temperature range, unless otherwise specified)

PARAMETER		SYMBOL	MIN.	NOM.	MAX.	UNIT
Power supply range	T_A = 0 ~ 70°C	V_S	1.8	-	5.5	V
	T_A = -40 ~ 125°C		2.0	-	5.5	
Operating ambient temperature		T_A	-40	-	125	°C

7 Specifications

7.3 ESD Ratings

ESD RATINGS		VALUE	UNIT
Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(4)	5000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(5)	2000	
	Machine model (MM), per JESD22-A115C	250	

(4) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

(5) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

7.4 Thermal Information

THERMAL METRIC(6)	SYMBOL	SOT-23-5L	SOP8	SOP14	DFNWB2×2-8L	UNIT
Junction-to-ambient thermal resistance	$R_{\Theta JA}$	192.3	125.0	115.7	94.7	°C/W
Reference maximum power dissipation (continuous)	$P_{D\ Ref}$	0.65	1.00	1.08	1.32	W

(6) T_A = 25°C, measured on evaluation board with 1oz. copper traces of minimum pad size, all device outputs were active.

7 Specifications

7.5 Electrical Characteristics

(V_S = (V+) - (V-) = 5.0V, T_A = 25°C, V_{CM} = V_S /2, V_O = V_S /2, and R_L = 10kΩ connected to V_S /2, unless otherwise noted. Boldface limits apply over the specified temperature range, T_A = −40 to +125°C.)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
OFFSET VOLTAGE						
Input offset voltage	V_{OS}	-	-	±2	±8	μV
Offset voltage drift	V_{OS} TC	T_A = −40 to +125°C	-	±5	±40	nV/°C
Power supply rejection ratio	PSRR	V_S = 2.0 to 5.5V, V_{CM} < (V+) −2V	112	126	-	dB
		T_A = −40 to +125°C	106	-	-	
INPUT VOLTAGE						
Common-mode voltage range	V_{CM}	-	(V-)−0.1	-	(V+)+0.1	V
Common-mode rejection ratio	CMRR	V_S = 5.5V, V_{CM} = −0.1 to 5.5V	112	130	-	dB
		V_{CM} = 0 to 5.3V, T_A = −40 to +125°C	106	-	-	
		V_S = 2.0V, V_{CM} = −0.1 to 2.0V	102	122	-	
		V_{CM} = 0 to 1.8V, T_A = −40 to +125°C	96	-	-	
INPUT BIAS CURRENT						
Input bias current	I_B	-	-	±70	-	pA
		T_A = +85°C	-	±150	-	
		T_A = +125°C	-	±700	-	
Input offset current	I_{OS}	-	-	±100	-	pA
NOISE						
Input voltage noise	E_n	f = 0.01 to 1Hz	-	0.1	-	μV_{PP}
		f = 0.1 to 10Hz	-	0.45	-	
Input voltage noise density	e_n	f = 10kHz	-	15	-	nV/√Hz
		f = 1kHz	-	19	-	
Input current noise density	I_n	f = 1kHz	-	10	-	fA/√Hz
INPUT IMPEDANCE						
Input resistance	R_{IN}	-	100	-	-	GΩ
Input capacitance	C_{IN}	Differential	-	2.0	-	pF
		Common mode	-	3.5	-	
OPEN-LOOP GAIN						
Open-loop voltage gain	A_{VOL}	R_L = 20kΩ, V_O = 0.05 to 3.5V	112	132	-	dB
		T_A = −40 to +125°C	106	-	-	
		R_L = 2kΩ, V_O = 0.15 to 3.5V	101	120	-	
		T_A = −40 to +125°C	95	-	-	

7 Specifications

7.5 Electrical Characteristics (conitnued)

(V_S = (V+) - (V-) = 5.0V, T_A = 25°C, V_{CM} = V_S /2, V_O = V_S /2, and R_L = 10kΩ connected to V_S /2, unless otherwise noted. Boldface limits apply over the specified temperature range, T_A = −40 to +125°C.)

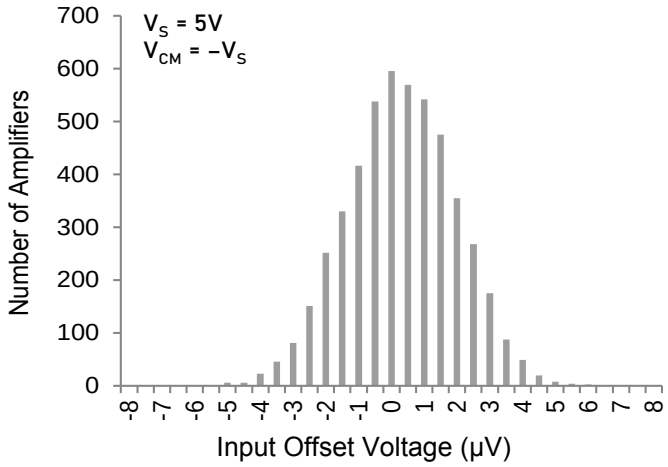
CHARACTERISTIC	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
FREQUENCY RESPONSE						
Gain bandwidth product	GBW	f = 1kHz	-	1.5	-	MHz
Slew rate	SR	G = +1, C_L = 10 pF, V_O = 1.5 to 3.5V	-	1.2	-	V/μs
Settling time	t_S	To 0.1%, G = +1, 1V step	-	1.2	-	μs
		To 0.01%, G = +1, 1V step	-	1.5	-	
Overload recovery time	t_{OR}	To 0.1%, V_{IN} x Gain > V_S	-	35	-	μs
OUTPUT						
High output voltage swing	V_{OH}	R_L = 20kΩ	-	(V+)–6	-	mV
		R_L = 2kΩ	(V+)–100	(V+)–60	-	
Low output voltage swing	V_{OL}	R_L = 20kΩ	-	(V-)+4	-	mV
		R_L = 2kΩ	-	(V-)+40	(V-)+66	
Open-loop output impedance	Z_{OUT}	f = 350kHz, I_O = 0	-	2	-	kΩ
Short-circuit current	I_{SC}	Source current through 10Ω	-	40	-	mA
		Sink current through 10Ω	-	50	-	
POWER SUPPLY						
Quiescent current (per amplifier)	I_Q	-	80	125	190	μA

7 Specifications

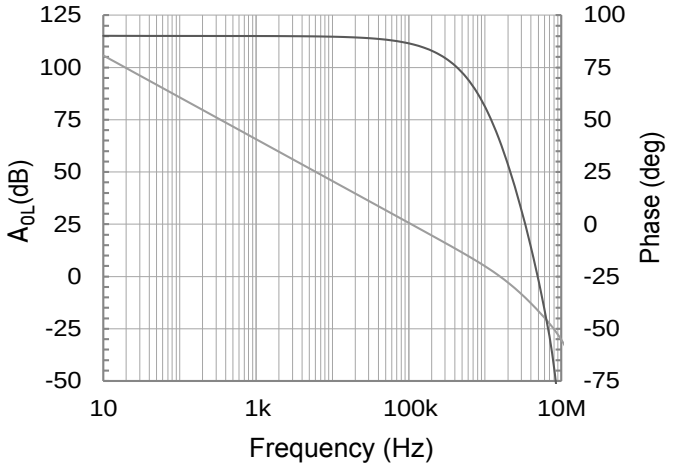
7.6 Typical Characteristics

At T_A = +25°C, V_S = ±2.5V, V_{CM} = V_S /2, R_L = 10kΩ connected to V_S /2, and C_L=100pF, unless otherwise noted.

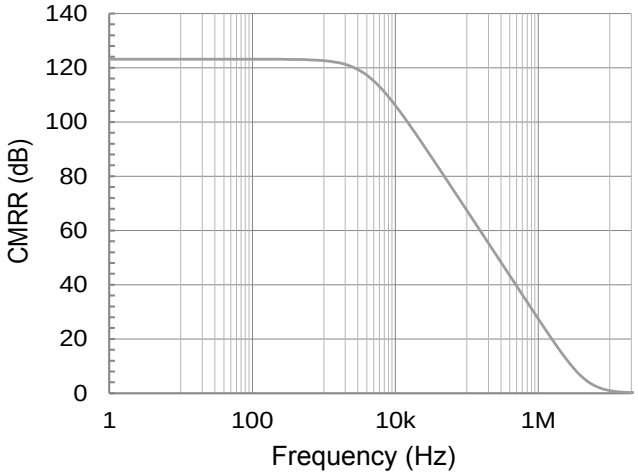
Input Offset Voltage Production Distribution



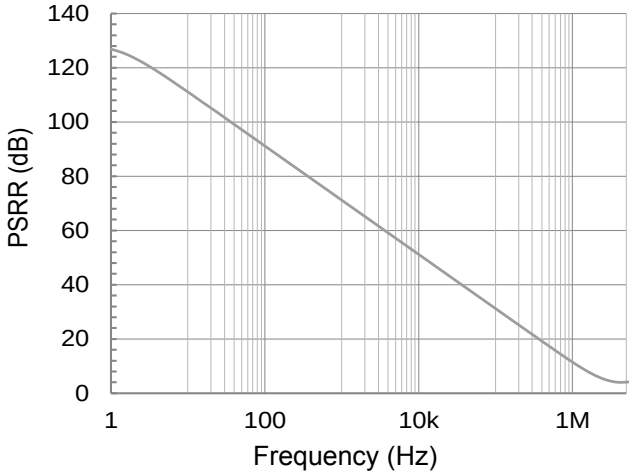
Open-loop Gain and Phase vs. Frequency



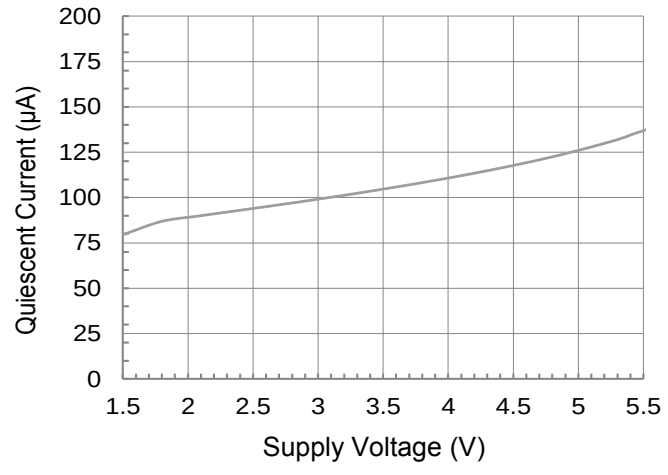
Common-mode Rejection Ratio vs. Frequency



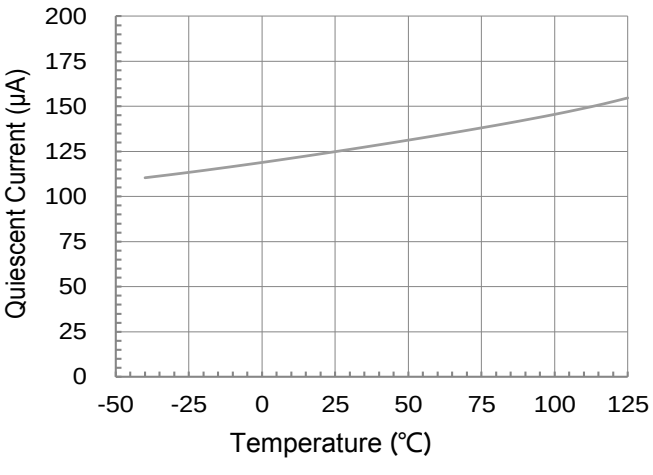
Power Supply Rejection Ratio vs. Frequency



Quiescent Current vs. Supply Voltage



Quiescent Current vs. Temperature

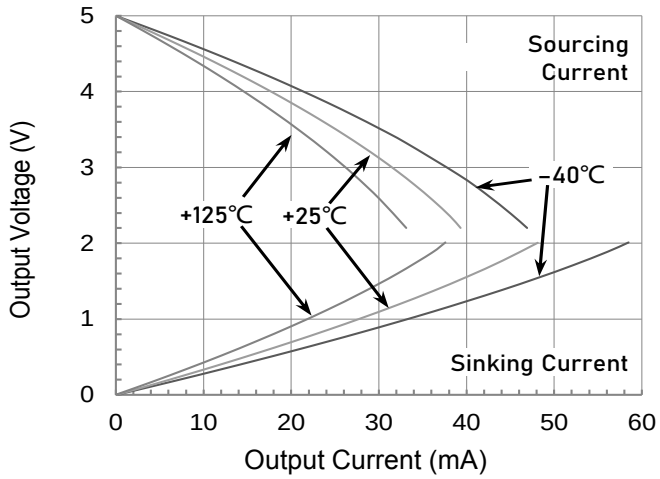


7 Specifications

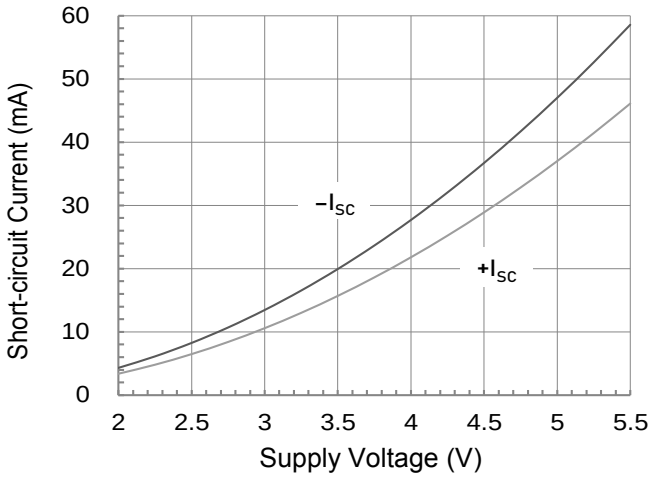
7.6 Typical Characteristics (continued)

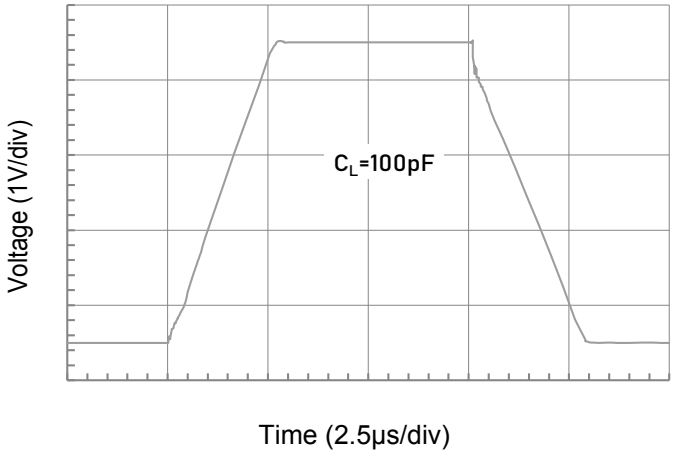
At T_A = +25°C, V_S = ±2.5V, V_{CM} = V_S /2, R_L = 10kΩ connected to V_S /2, and C_L=100pF, unless otherwise noted.

Output Voltage Swing vs. Output Current

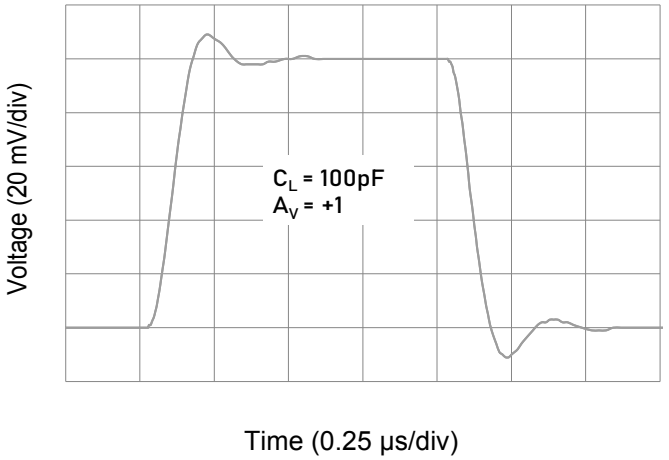


Short-circuit Current vs. Supply Voltage





Small Signal Step Response (100mV Step)



8 Detail Description

8.1 Description

The CJOA855x family of amplifiers provides input offset voltage correction for very low offset and drift through the use of patented fast step response chopper stabilized techniques. This method constantly measures and compensates the input offset, eliminating drift over time and temperature and the effect of 1/f noise. This design breakthrough allows the combination of a gain bandwidth product of 1.5MHz and a high slew rate of 1.2V/μs, while only drawing 125μA supply current. These devices are unity gain stable and have good Power Supply Rejection Ratio (PSRR) and Common Mode Rejection Ratio (CMRR).

8.2 Feature Description

Input Voltage

The input common-mode voltage range of the CJOA855x series extends 100mV beyond the negative and positive supply rails. This performance is achieved with a complementary input stage: an N-channel input differential pair in parallel with a P-channel differential pair. The N-channel pair is active for input voltages close to the positive rail, typically (V+)–1.4V to the positive supply, whereas the P-channel pair is active for inputs from 100mV below the negative supply to approximately (V+)–1.4V. There is a small transition region, typically (V+)–1.2V to (V+)–1V, in which both pairs are on. This 200mV transition region can vary up to 200mV with process variation. Thus, the transition region (both stages on) can range from (V+)–1.4V to (V+)–1.2V on the low end, up to (V+)–1V to (V+)–0.8V on the high end. Within this transition region, PSRR, CMRR, offset voltage, offset drift, and THD can be degraded compared to device operation outside this region.

The typical input bias current of the CJOA855x during normal operation is approximately 70pA. In overdriven conditions, the bias current can increase significantly. The most common cause of an overdriven condition occurs when the operational amplifier is outside of the linear range of operation. When the output of the operational amplifier is driven to one of the supply rails, the feedback loop requirements cannot be satisfied and a differential input voltage develops across the input pins. This differential input voltage results in activation of parasitic diodes inside the front-end input chopping switches that combine with electromagnetic interference (EMI) filter resistors to create the equivalent circuit. Notice that the input bias current remains within specification in the linear region.

Internal Offset Correction

The CJOA855x operational amplifiers use an auto-calibration technique with a time-continuous 500kHz operational amplifier in the signal path. This amplifier is zero-corrected every 2μs using a proprietary technique. Upon power up, the amplifier requires approximately 100μs to achieve specified V_{OS} accuracy. This design has no aliasing or flicker noise.

8 Detail Description

8.2 Feature Description (continued)

Overload Recovery

Overload recovery is defined as the time required for the operational amplifier output to recover from a saturated state to a linear state. The output devices of the operational amplifier enter a saturation region when the output voltage exceeds the rated operating voltage, either because of the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return back to the linear state. After the charge carriers return back to the linear state, the device begins to slew at the specified slew rate. Thus, the propagation delay in case of an overload condition is the sum of the overload recovery time and the slew time. The overload recovery time for the CJOA855x family is approximately 35μs.

EMI Rejection Ratio

Circuit performance is often adversely affected by high frequency EMI. When the signal strength is low and transmission lines are long, an op-amp must accurately amplify the input signals. However, all op-amp pins — the non-inverting input, inverting input, positive supply, negative supply, and output pins —are susceptible to EMI signals. These high frequency signals are coupled into an op-amp by various means, such as conduction, near field radiation, or far field radiation. For example, wires and printed circuit board (PCB) traces can act as antennas and pick up high frequency EMI signals.

Amplifiers do not amplify EMI or RF signals due to their relatively low bandwidth. However, due to the nonlinearities of the input devices, op-amps can rectify these out of band signals. When these high frequency signals are rectified, they appear as a dc offset at the output.

The CJOA855x op-amps have integrated EMI filters at their input stage. A mathematical method of measuring EMIRR is defined as follows:

$$EMIRR = 20\ log\left(V_{IN_PEAK}/\Delta V_{OS}\right)$$

9 Application and Implementation

9.1 Application Information

The CJOA855x operational amplifiers are unity-gain stable and free from unexpected output phase reversal. These devices use a proprietary auto-calibration technique to provide low offset voltage and very low drift over time and temperature. For lowest offset voltage and precision performance, optimize circuit layout and mechanical conditions. Avoid temperature gradients that create thermoelectric (Seebeck) effects in the thermocouple junctions formed from connecting dissimilar conductors. Cancel these thermally-generated potentials by assuring they are equal on both input terminals. Other layout and design considerations include:

- Use low thermoelectric-coefficient conditions (avoid dissimilar metals).
- Thermally isolate components from power supplies or other heat sources.
- Shield operational amplifier and input circuitry from air currents, such as cooling fans.

Following these guidelines reduces the likelihood of junctions being at different temperatures, which can cause thermoelectric voltages of 0.1μV/°C or higher, depending on materials used.

9.2 Typical Application Circuits

Input EMI Filter and Clamp Circuit

Figure 9-1 shows the input EMI filter and clamp circuit. The CJOA855x op-amps have internal ESD protection diodes (D1, D2, D3, and D4) that are connected between the inputs and each supply rail. These diodes protect the input transistors in the event of electrostatic discharge and are reverse biased during normal operation. This protection scheme allows voltages as high as approximately 500mV beyond the rails to be applied at the input of either terminal without causing permanent damage. See the table of Absolute Maximum Ratings for more information.

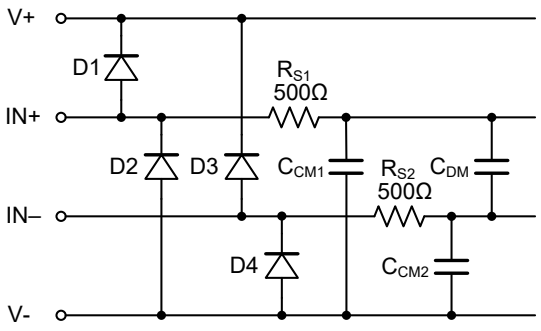


Figure 9-1. Input EMI Filter and Clamp Circuit

Operational amplifiers vary in susceptibility to EMI. If conducted EMI enters the operational amplifier, the dc offset at the amplifier output can shift from its nominal value when EMI is present. This shift is a result of signal rectification associated with the internal semiconductor junctions. Although all operational amplifier pin functions can be affected by EMI, the input pins are likely to be the most susceptible. The EMI filter of the CJOA855x family is composed of two 5kΩ input series resistors (R_{S1} and R_{S2}), two common-mode capacitors (C_{CM1} and C_{CM2}), and a differential capacitor (C_{DM}). These RC networks set the −3dB low-pass cutoff frequencies at 35MHz for common-mode signals, and at 22MHz for differential signals.

9 Application and Implementation

9.2 Typical Application Circuits (continued)

Capacitive Load and Stability

The CJOA855x family can safely drive capacitive loads of up to 500pF in any configuration. As with most amplifiers, driving larger capacitive loads than specified may cause excessive overshoot and ringing, or even oscillation. A heavy capacitive load reduces the phase margin and causes the amplifier frequency response to peak. Peaking corresponds to over-shooting or ringing in the time domain. Therefore, it is recommended that external compensation be used if the CJOA855x op-amps must drive a load exceeding 500pF. This compensation is particularly important in the unity-gain configuration, which is the worst case for stability.

A quick and easy way to stabilize the op-amp for capacitive load drive is by adding a series resistor, R_{ISO}, between the amplifier output terminal and the load capacitance, as shown in Figure 9-2. R_{ISO} isolates the amplifier output and feedback network from the capacitive load. The bigger the R_{ISO} resistor value, the more stable V_{OUT} will be. Note that this method results in a loss of gain accuracy because R_{ISO} forms a voltage divider with the R_L.

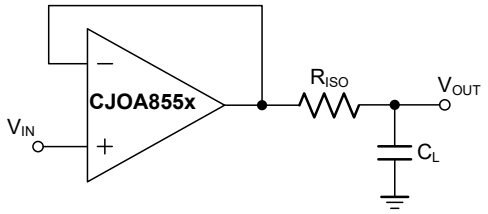


Figure 9-2. Indirectly Driving Heavy Capacitive Load

An improvement circuit is shown in Figure 9-3. It provides DC accuracy as well as AC stability. The RF provides the DC accuracy by connecting the inverting signal with the output.

The CF and RISO serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop.

For no-buffer configuration, there are two others ways to increase the phase margin: (a) by increasing the amplifier's gain, or (b) by placing a capacitor in parallel with the feedback resistor to counteract the parasitic capacitance associated with inverting node.

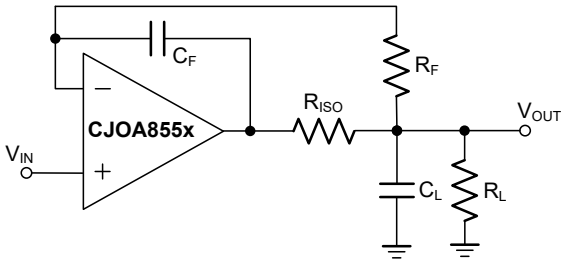


Figure 9-3. Indirectly Driving Heavy Capacitive Load with DC Accuracy

Input-to-Output Coupling

To minimize capacitive coupling, the input and output signal traces should not be parallel. This helps reduce unwanted positive feedback.

9 Application and Implementation

9.2 Typical Application Circuits (continued)

Precision Low-side Current Shunt Sensing

Many applications require the sensing of signals near the positive or negative rails. Current shunt sensing is one such application and is mostly used for feedback control systems. It is also used in a variety of other applications, including power metering, battery fuel gauging, and feedback controls in industrial applications. In such applications, it is desirable to use a shunt with very low resistance to minimize series voltage drop. This configuration not only minimizes wasted power, but also allows the measurement of high currents while saving power.

A typical shunt may be 100mΩ. At a measured current of 1A, the voltage produced from the shunt is 100mV, and the amplifier error sources are not critical. However, at low measured current in the 1mA range, the 100μV generated across the shunt demands a very low offset voltage and drift amplifier to maintain absolute accuracy.

The unique attributes of a zero drift amplifier provide a solution. Figure 9-4 shows a low-side current sensing circuit using the CJOA8551/CJOA8552. The CJOA8551/CJOA8552 are configured as difference amplifiers with a gain of 1000. Although the CJOA8551/CJOA8552 have high CMRR, the CMRR of the system is limited by the external resistors. Therefore, the key to high CMRR for the system is resistors that are well matched from both the resistive ratio and relative drift, where R1/R2 =R3/R4. The transfer function is given by:

$$V_{OUT} = V_{SHUNT} \times Gain_{Diff_Amp} = (R_{SHUNT} \times I_{LOAD}) \times (R2/R1) = 100 \times I_{LOAD}$$

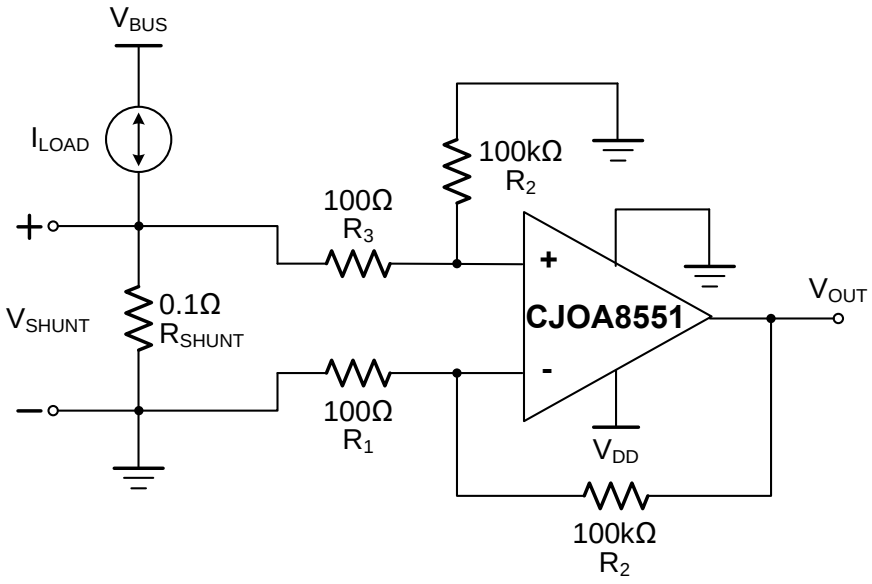


Figure 9-4. Low-Side Current Sensing Circuit

Any unused channel of the CJOA8551/CJOA8552 must be configured in unity gain with the input common-mode voltage tied to the midpoint of the power supplies.

Bidirectional Current-Sensing

This single-supply, low-side, bidirectional current-sensing solution detects load currents from –1A to +1A. The single-ended output spans from 110mV to 3.19V. This design uses the CJOA855x because of its low offset voltage and rail-to-rail input and output. One of the amplifiers is configured as a difference amplifier and the other amplifier provides the reference voltage.

Figure 9-5 shows the solution. This solution has the following requirements:

- Supply voltage: 3.3V
- Input: –1A to +1A
- Output: 1.65V±1.54V (110mV to 3.19V)

9 Application and Implementation

9.2 Typical Application Circuits (continued)

Bidirectional Current-Sensing (continued)

There are two types of errors in this design: offset and gain. Gain errors are introduced by the tolerance of the shunt resistor and the ratios of R_4 to R_3 and, similarly, R_2 to R_1. Offset errors are introduced by the voltage divider (R_5 and R_6) and how closely the ratio of R_4/R_3 matches R_2/R_1. The latter value affects the CMRR of the difference amplifier, ultimately translating to an offset error.

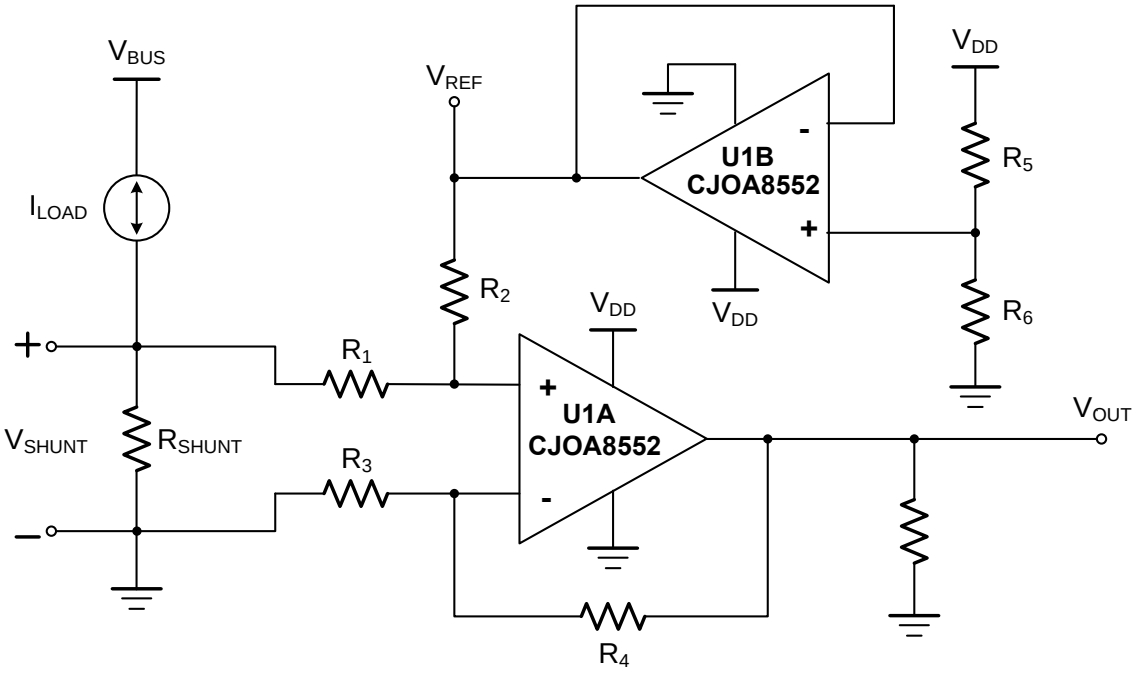


Figure 9-5. Bidirectional Current-Sensing Schematic

The load current, I_{LOAD}, flows through the shunt resistor (R_{SHUNT}) to develop the shunt voltage, V_{SHUNT}. The shunt voltage is then amplified by the difference amplifier consisting of U1A and R_1 through R_4.The gain of the difference amplifier is set by the ratio of R_4 to R_3. To minimize errors, set $R_2 = R_4$ and $R_1 = R_3$. The reference voltage, V_{REF}, is supplied by buffering a resistor divider using U1B. The transfer function is given by Equation 1.

$$V_{OUT} = V_{SHUNT} \times Gain_{Diff_Amp} + V_{REF}$$

Where

- $V_{SHUNT} = I_{LOAD} \times R_{SHUNT}$
- $Gain_{Diff_{Amp}} = R_4/R_3$
- $V_{REF} = V_{DD} \times [R_6/(R_5 + R_6)]$ (1)

There are two types of errors in this design: offset and gain. Gain errors are introduced by the tolerance of the shunt resistor and the ratios of R_4 to R_3 and, similarly, R_2 to R_1. Offset errors are introduced by the voltage divider (R_5 and R_6) and how closely the ratio of R_4/R_3 matches R_2/R_1. The latter value affects the CMRR of the difference amplifier, ultimately translating to an offset error.

The value of V_{SHUNT} is the ground potential for the system load because V_{SHUNT} is a low-side measurement. Therefore, a maximum value must be placed on V_{SHUNT}. In this design, the maximum value for V_{SHUNT} is set to 100mV. Equation 2 calculates the maximum value of the shunt resistor given a maximum shunt voltage of 100mV and maximum load current of 1A.

$$R_{SHUNT(MAX)} = R_{SHUNT(MAX)}/I_{LOAD(MAX)} = 100mV/1A = 100m\Omega \quad (2)$$

9 Application and Implementation

9.2 Typical Application Circuits (continued)

Bidirectional Current-Sensing (continued)

The tolerance of R_{SHUNT} is directly proportional to cost. For this design, a shunt resistor with a tolerance of 0.5%was selected. If greater accuracy is required, select a 0.1% resistor or better.

The load current is bidirectional; therefore, the shunt voltage range is –100mV to +100mV. This voltage is divided down by R_1 and R_2 before reaching the operational amplifier, U1A. Take care to ensure that the voltage present at the non-inverting node of U1A is within the common-mode range of the device. Therefore, use an operational amplifier, such as the CJOA8551, that has a common-mode range that extends below the negative supply voltage. Finally, to minimize offset error, note that the CJOA8551 has a typical offset voltage of merely ±2Mv (±8μV maximum). Given a symmetric load current of –1A to +1A, the voltage divider resistors (R_5 and R_6) must be equal. To be consistent with the shunt resistor, a tolerance of 0.5% was selected. To minimize power consumption, 10kΩ resistors were used.

To set the gain of the difference amplifier, the common-mode range and output swing of the CJOA8551 must be considered. Equation 3 and Equation 4 depict the typical common-mode range and maximum output swing, respectively, of the CJOA8551 given a 3.3V supply.

- $-100mV < V_{CM} < 3.4V$ (3)
- $100mV < V_{OUT} < 3.2V$ (4)

The gain of the difference amplifier can now be calculated as shown in Equation 5.

$$Gain_{Diff_{Amp}} = \left(V_{OUT_{MAX}} - V_{OUT_{MIN}}\right)/[R_{SHUNT} \times (I_{MAX} - I_{MIN})] = (3.2V - 100mV)/100m\Omega \times [1A - (-1A)] = 15.5V/V \quad (5)$$

The resistor value selected for R_1 and R_3 was 1kΩ.15.4kΩ was selected for R_2 and R_4 because this number is the nearest standard value. Therefore, the ideal gain of the difference amplifier is 15.4V/V.

The gain error of the circuit primarily depends on R_1 through R_4. As a result of this dependence, 0.1% resistors were selected. This configuration reduces the likelihood that the design requires a two-point calibration. A simple one-point calibration, if desired, removes the offset errors introduced by the 0.5% resistors.

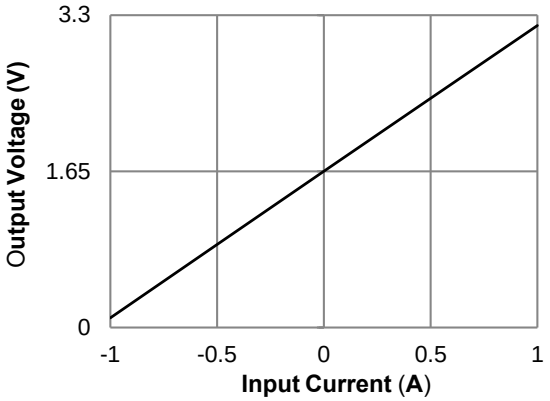


Figure 9-6. Bidirectional Current-Sensing Circuit Performance: Output Voltage vs. Input Current

9 Application and Implementation

9.2 Typical Application Circuits (continued)

High-side Voltage-to-Current (V-I) Converter

An improvement circuit is shown in Figure 9-7. It provides DC accuracy as well as AC stability. The RF provides the DC accuracy by connecting the inverting signal with the output.

The circuit shown in Figure 9-7 is a high-side voltage-to-current (V-I) converter. It translates in input voltage of 0V to 2V to and output current of 0mA to 100mA.

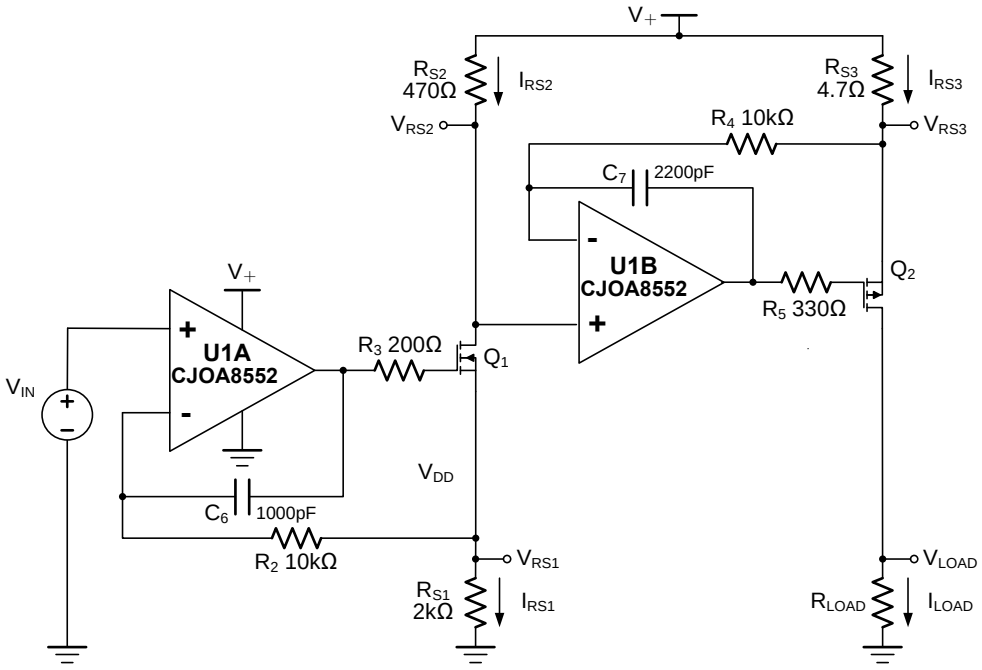


Figure 9-7. Bidirectional Current-Sensing Schematic

The design requirements are as follows:

- Supply Voltage: 5V DC
- Input: 0V to 2V DC
- Output: 0mA to 100mA DC

The V-I transfer function of the circuit is based on the relationship between the input voltage, V_{IN}, and the three current sensing resistors, R_{S1}, R_{S2}, and R_{S3}. The relationship between V_{IN} and R_{S1} determines the current that flows through the first stage of the design. The current gain from the first stage to the second stage is based on the relationship between R_{S2} and R_{S3}.

For a successful design, pay close attention to the dc characteristics of the operational amplifier chosen for the application. To meet the performance goals, this application benefits from an operational amplifier with low offset voltage, low temperature drift, and rail-to-rail output. The CJOA8552 CMOS operational amplifier is a high-precision, typically 2μV offset, 5nV/°C drift amplifier optimized for low-voltage, single-supply operation with an output swing to within 15mV (at RL =10kΩ) of the positive rail. The CJOA8552 family uses chopping techniques to provide low initial offset voltage and near-zero drift over time and temperature. Low offset voltage and low drift reduce the offset error in the system, making these devices appropriate for precise dc control. The rail-to-rail output stage of the CJOA8552 ensures that the output swing of the operational amplifier is able to fully control the gate of the MOSFET devices within the supply rails.

Figure 9-8 shows the measured transfer function for this circuit. The low offset voltage and offset drift of the CJOA8552 facilitate excellent dc accuracy for the circuit.

9 Application and Implementation

9.2 Typical Application Circuits (continued)

High-side Voltage-to-Current (V-I) Converter (continued)

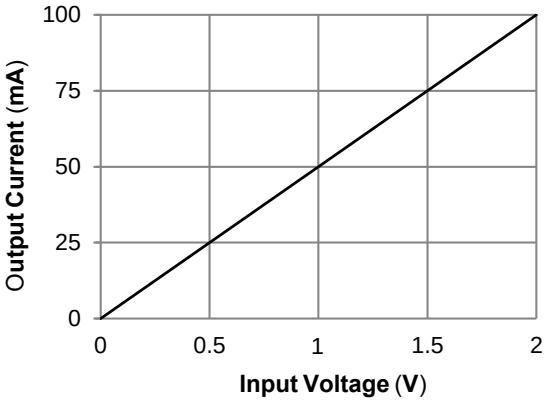


Figure 9-8. Bidirectional Current-Sensing Schematic

Single-supply Instrumentation Amplifier

The extremely low offset voltage and drift, high open-loop gain, high common-mode rejection, and high power supply rejection of the CJOA8551/CJOA8552 make them excellent op-amp choices as discrete, single-supply instrumentation amplifiers.

Figure 9-9 shows the classic 3-op-amp instrumentation amplifier using the CJOA8551/CJOA8552. The key to high CMRR for the instrumentation amplifier are resistors that are well matched for both the resistive ratio and relative drift. For true difference amplification, matching of the resistor ratio is very important, where:

- $R_5/R_2 = R_6/R_4$
- $R_{G1} = R_{G2}, R_1 = R_3, R_2 = R_4, R_5 = R_6$
- $V_{OUT} = (V_{IN1} - V_{IN2}) \times (1 + R_1/R_{G1}) \times (R_5/R_2)$

The resistors are important in determining the performance over manufacturing tolerances, time, and temperature. Assuming a perfect unity-gain difference amplifier with infinite common-mode rejection, a 1% tolerance resistor matching results in only 34dB of common-mode rejection. Therefore, at least 0.01% or better resistors are recommended.

To build a discrete instrumentation amplifier with external resistors without compromising on noise, pay close attention to the resistor values chosen. R_{G1} and R_{G2} each have thermal noise that is amplified by the total noise gain of the instrumentation amplifier and, therefore, a sufficiently low value must be chosen to reduce thermal noise contribution at the output while still providing an accurate measurement.

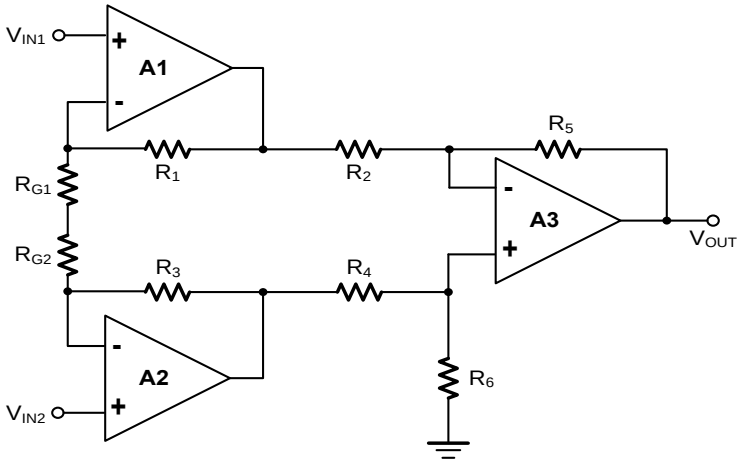


Figure 9-9. Discrete 3-Op-amp Instrumentation Amplifier

9 Application and Implementation

9.2 Typical Application Circuits (continued)

Single-supply Instrumentation Amplifier (continued)

Figure 9-10 shows the external resistors noise contribution referred to the output.

Resistor	Value	Resistor Thermal Noise	Thermal Noise Referred to Output
R_{G1}	0.4kΩ	2.57 nV/√Hz	128.30 nV/√Hz
R_{G2}	0.4kΩ	2.57 nV/√Hz	128.30 nV/√Hz
R_1	10kΩ	12.83 nV/√Hz	25.66 nV/√Hz
R_2	10kΩ	12.83 nV/√Hz	25.66 nV/√Hz
R_3	10kΩ	12.83 nV/√Hz	25.66 nV/√Hz
R_4	10kΩ	12.83 nV/√Hz	25.66 nV/√Hz
R_5	20kΩ	18.14 nV/√Hz	18.14 nV/√Hz
R_6	20kΩ	18.14 nV/√Hz	18.14 nV/√Hz

Figure 9-10. Thermal Noise Contribution Example

Note that A1 and A2 have a high gain of $1 + R_1/R_{G1}$. Therefore, use a high precision, low offset voltage and low noise amplifier forA1and A2, such as the CJOA8551/CJOA8552. Conversely, A3 operates at a much lower gain and has a different set of op-amp requirements. Its input noise, referred to the overall instrumentation amplifier input, is divided by the first stage gain and is not as important. Note that the input offset voltage and the input voltage noise of the amplifiers are also amplified by the overall noise gain.

Any unused channel of the CJOA8551/CJOA8552 must be configured in unity gain with the input common-mode voltage tied to the midpoint of the power supplies.

Understanding how noise impacts a discrete instrumentation amplifier or a difference amplifier (the second stage of a 3-op-amp instrumentation amplifier) is important, because they are commonly used in many different applications.

Load Cell (Strain Gage) Sensor Signal Conditioning

The CJOA8552, with its ultralow offset, drift, and noise, is well suited to signal condition a low level sensor output with high gain and accuracy. A weigh scale (load cell) is an example of an application with such requirements. Figure 9-11 shows a configuration for a single-supply, precision, weigh scale measurement system. The CJOA8552 is used at the front end for amplification of the low level signal from the load cell.

Current flowing through a PCB trace produces an IR voltage drop; with longer traces, this voltage drop can be several millivolts or more, introducing a considerable error. A 1inch long, 0.005inch wide trace of 1oz copper has a resistance of approximately 100mΩ at room temperature. With a load current of 10mA, the resistance can introduce a 1mV error.

Therefore, a 6-wire load cell is used in the circuit. The load cell has two sense pins, in addition to excitation, ground, and two output connections. The sense pins are connected to the high side (excitation pin) and low side (ground pin) of the Wheatstone bridge. The voltage across the bridge can then be accurately measured regardless of voltage drop due to wire resistance. The two sense pins are also connected to the analog-to-digital converter (ADC) reference inputs for a ratio-metric configuration that is immune to low frequency changes in the power supply excitation voltage.

9 Application and Implementation

9.2 Typical Application Circuits (continued)

Load Cell (Strain Gage) Sensor Signal Conditioning (continued)

The CJOA8552 is configured as the first stage of a 3-op-amp instrumentation amplifier to amplify the low level amplitude signal from the load cell by a factor of $1+2R_1/R_G$. Capacitors C_1 and C_2 are placed in the feedback loops of the amplifiers and interact with R_1 and R_2 to perform low-pass filtering. This filtering limits the amount of noise entering the Σ-Δ ADC. In addition, C_3, C_4, C_5, R_3 and R_4 provide further common-mode and differential mode filtering to reduce noise and unwanted signals.

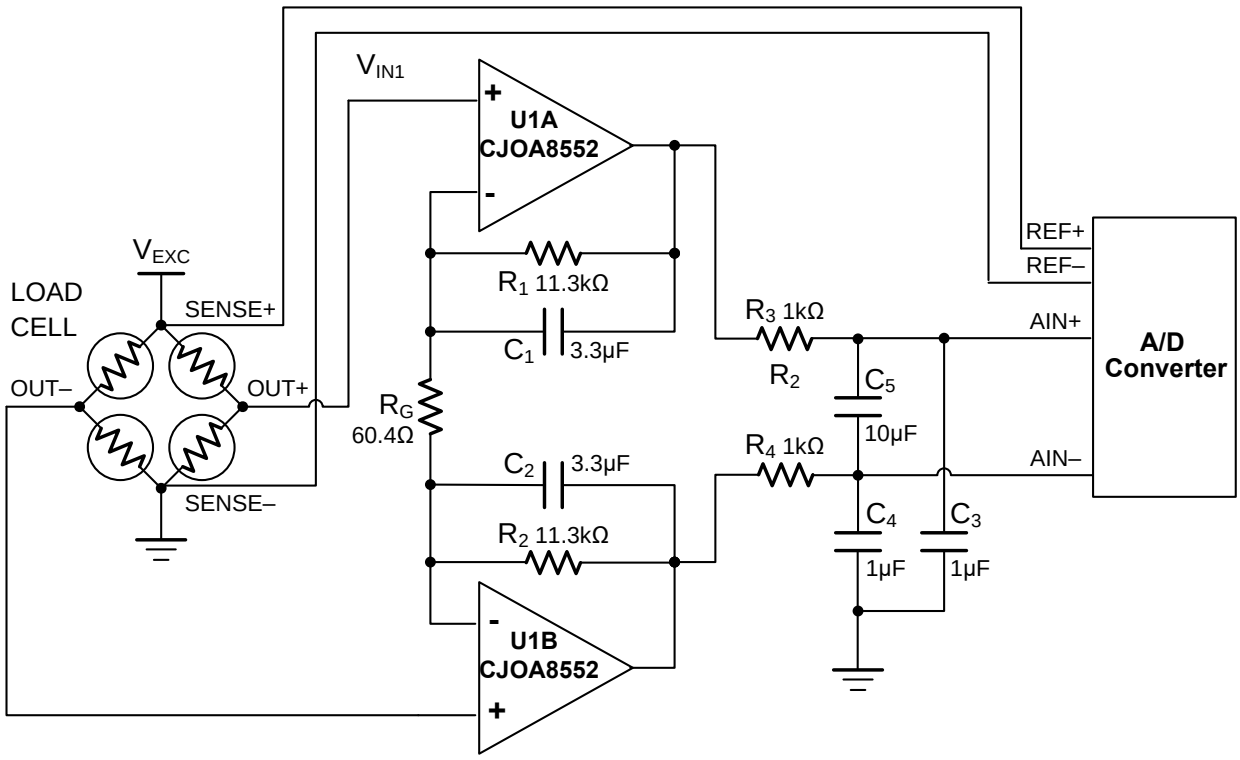


Figure 9-11. Precision Weigh Scale Measurement System

9.3 Power Supply Recommendations

The CJOA855x family is fully specified and ensured for operation from 2.0V to 5.5V (±1.0V to ±2.75V). In addition, many specifications apply from −40°C to +125°C. Parameters that vary significantly with operating voltages or temperature are illustrated in the Typical Characteristics graphs.

NOTE: Supply voltages (V+ to V-) higher than +10V can permanently damage the device.

9 Application and Implementation

9.4 Layout Guidelines

To achieve the maximum performance of the extremely high input impedance and low offset voltage of the CJOA855x op-amps, care is needed in laying out the circuit board. The PCB surface must remain clean and free of moisture to avoid leakage currents between adjacent traces. Surface coating of the circuit board reduces surface moisture and provides a humidity barrier, reducing parasitic resistance on the board. The use of guard rings around the amplifier inputs further reduces leakage currents. Figure 9-12 shows proper guard ring configuration and the top view of a surface-mount layout. The guard ring does not need to be a specific width, but it should form a continuous loop around both inputs. By setting the guard ring voltage equal to the voltage at the non-inverting input, parasitic capacitance is minimized as well. For further reduction of leakage currents, components can be mounted to the PCB using Teflon standoff insulators.

Other potential sources of offset error are thermoelectric voltages on the circuit board. This voltage, also called Seebeck voltage, occurs at the junction of two dissimilar metals and is proportional to the temperature of the junction. The most common metallic junctions on a circuit board are solder-to-board trace and solder-to-component lead. If the temperature of the PCB at one end of the component is different from the temperature at the other end, the resulting Seebeck voltages are not equal, resulting in a thermal voltage error.

This thermocouple error can be reduced by using dummy components to match the thermoelectric error source. Placing the dummy component as close as possible to its partner ensures both Seebeck voltages are equal, thus canceling the thermocouple error. Maintaining a constant ambient temperature on the circuit board further reduces this error. The use of a ground plane helps distribute heat throughout the board and reduces EMI noise pickup.

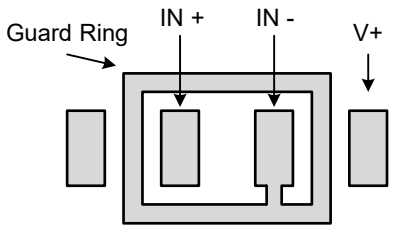
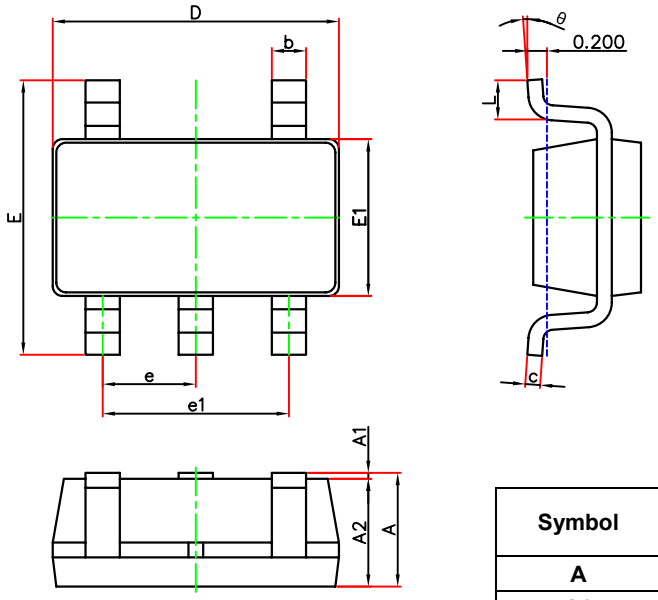


Figure 9-12. Guard Ring

10 Mechanical Information

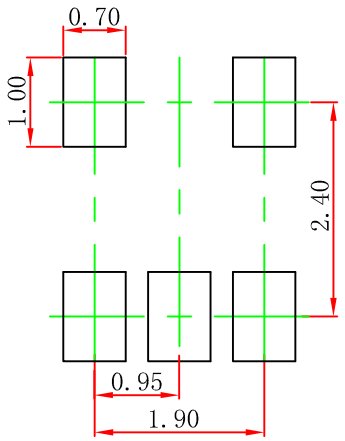
10.1 SOT-23-5L Mechanical Information

SOT-23-5L Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.000	1.200	0.039	0.047
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	2.600	3.000	0.102	0.118
E1	1.500	1.700	0.059	0.067
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

SOT-23-5L Suggested Pad Layout



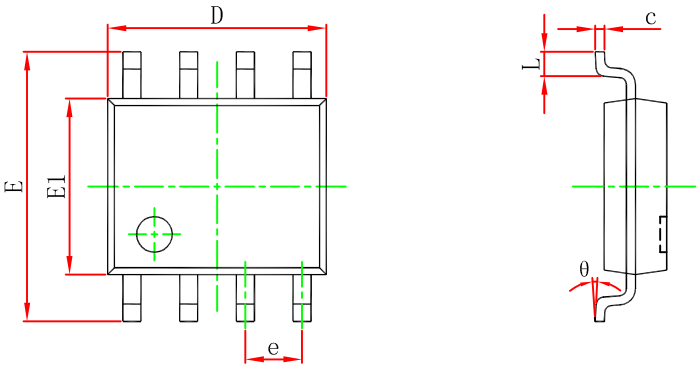
Note:

1. Controlling dimension: in millimeters.
2. General tolerance: ±0.05mm.
3. The pad layout is for reference purpose only.

10 Mechanical Information

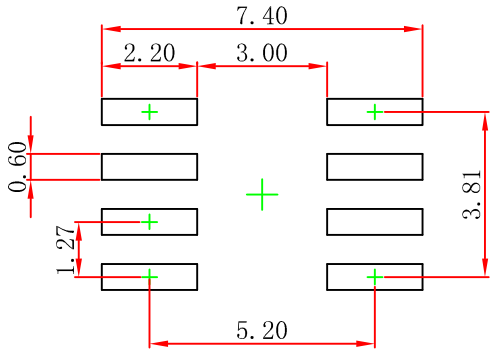
10.2 SOP8 Mechanical Information

Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	**Max**	**Min**	**Max**
A	1.370	1.670	0.054	0.066
A1	0.070	0.250	0.003	0.010
A2	1.350	1.550	0.053	0.061
b	0.300	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
e	1.270（BSC）		0.050（BSC）	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

SOP8 Suggest Pad Layout



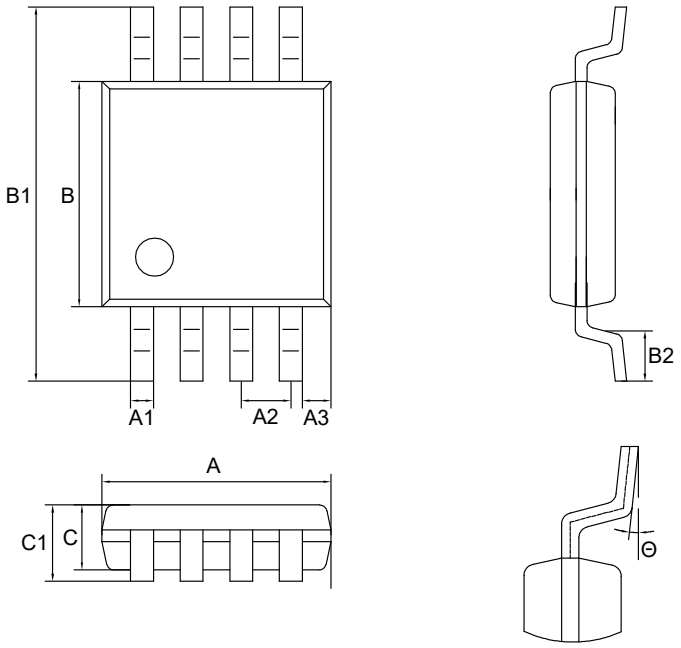
NOTE:

1. Controlling dimension: in millimeters.
2. General tolerance: ±0.05mm.
3. The pad layout is for reference purposes only.

10 Mechanical Information

10.3 MSOP8 Mechanical Information

Outline Dimensions

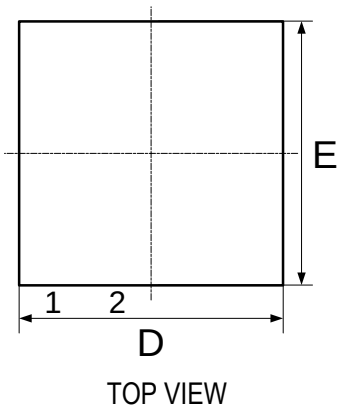


SYMBOL	DISMENSIONS IN MILLIMETERS			DISMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	2.900	3.000	3.100	0.114	0.118	0.122
A1	0.280	-	0.350	0.011	-	0.014
A2	0.650 TYP.			0.026 TYP.		
B	2.900	3.000	3.100	0.114	0.118	0.122
B1	4.700	-	5.100	0.185	-	0.201
B2	0.450	0.600	0.750	0.018	0.024	0.030
C	0.750	0.850	0.950	0.030	0.033	0.037
C1	-	-	1.100	-	-	0.043
Θ	0°	-	6°	0°	-	6°

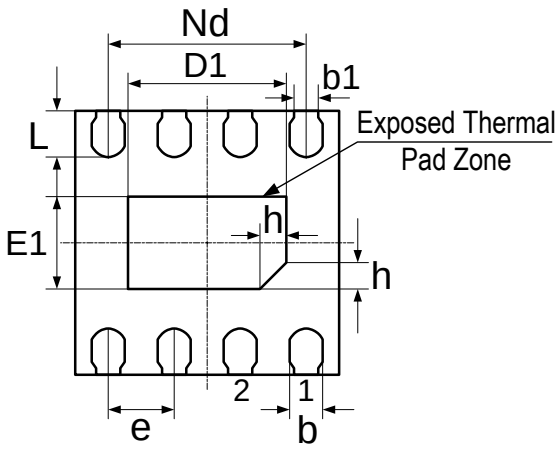
10 Mechanical Information

10.4 DFNWB2×2-8L Mechanical Information

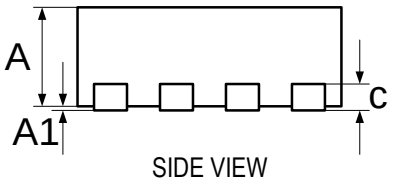
Outline Dimensions



TOP VIEW



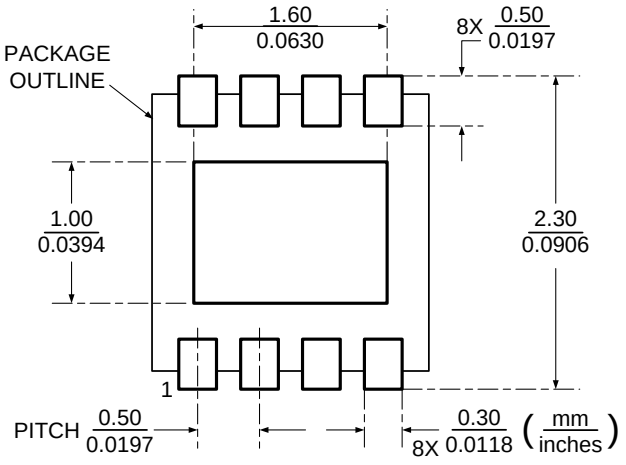
BOTTOM VIEW



SIDE VIEW

SYMBOL	DISMENSIONS IN MILLIMETERS			DISMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.700	0.750	0.800	0.028	0.030	0.031
A1	-	0.020	0.050	-	0.001	0.002
b	0.200	0.250	0.300	0.008	0.010	0.012
b1	0.180 Bsc.			0.007 Bsc.		
c	0.180	0.200	0.250	0.007	0.008	0.010
D	1.900	2.000	2.100	0.075	0.079	0.083
D2	1.100	1.200	1.300	0.043	0.047	0.051
Nd	1.500 Bsc.			0.059 Bsc.		
E	1.900	2.000	2.100	0.075	0.079	0.083
E1	0.600	0.700	0.800	0.024	0.028	0.031
e	0.500 Bsc.			0.020 Bsc.		
L	0.300	0.350	0.400	0.012	0.014	0.016
h	0.150	0.200	0.250	0.006	0.008	0.010

DFNWB2×2-8L Suggest Pad Layout



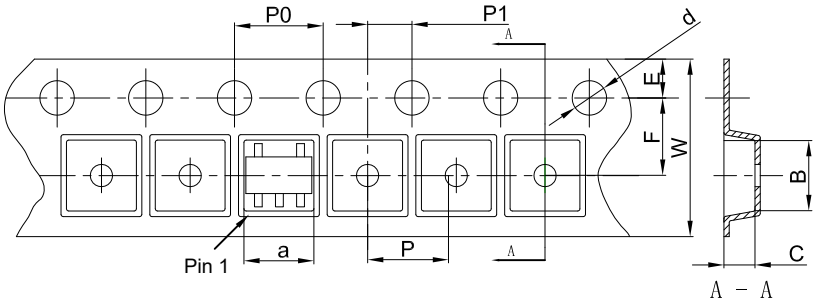
NOTE:

1. Controlling dimension: in millimeters.
2. General tolerance: ±0.05mm.
3. The pad layout is for reference purposes only.

11 Packaging Information

11.1 SOT-23-5L Tape and Reel Information

SOT-23-5L Tape and Reel Information

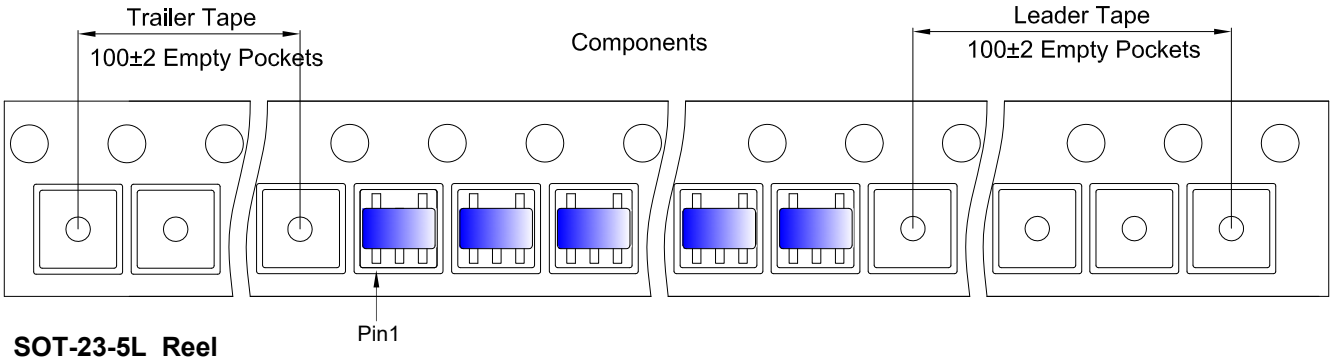


Packaging Description:

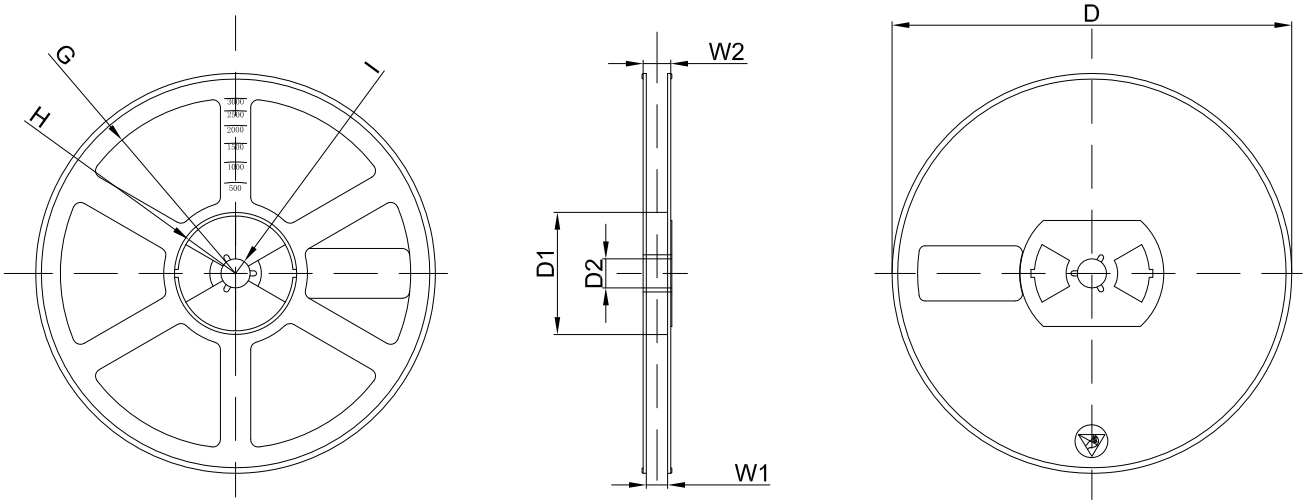
SOT-23-5L parts are shipped in tape. The carrier tape is made from a dissipative (carbon filled) polycarbonate resin. The cover tape is a multilayer film (Heat Activated Adhesive in nature) primarily composed of polyester film, adhesive layer, sealant, and anti-static sprayed agent. These reeled parts in standard option are shipped with 3,000 units per 7" or 18.0cm diameter reel. The reels are clear in color and is made of polystyrene plastic (anti-static coated).

Dimensions are in millimeter										
Pkg type	a	B	C	d	E	F	P0	P	P1	W
SOT-23-5L	3.17	3.23	1.37	Ø1.55	1.75	3.50	4.00	4.00	2.00	8.00

SOT-23-5L Tape Leader and Trailer



SOT-23-5L Reel



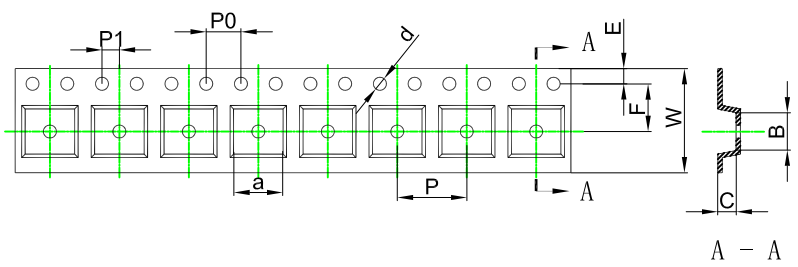
Dimensions are in millimeter								
Reel Option	D	D1	D2	G	H	I	W1	W2
7"Dia	Ø180.00	60.00	13.00	R78.00	R25.60	R6.50	9.50	13.10

REEL	Reel Size	Box	Box Size(mm)	Carton	Carton Size(mm)	G.W.(kg)
3000 pcs	7 inch	30,000 pcs	203×203×195	120,000 pcs	438×438×220	

11 Packaging Information

11.2 SOP8 Tape and Reel Information

Embossed Carrier Tape



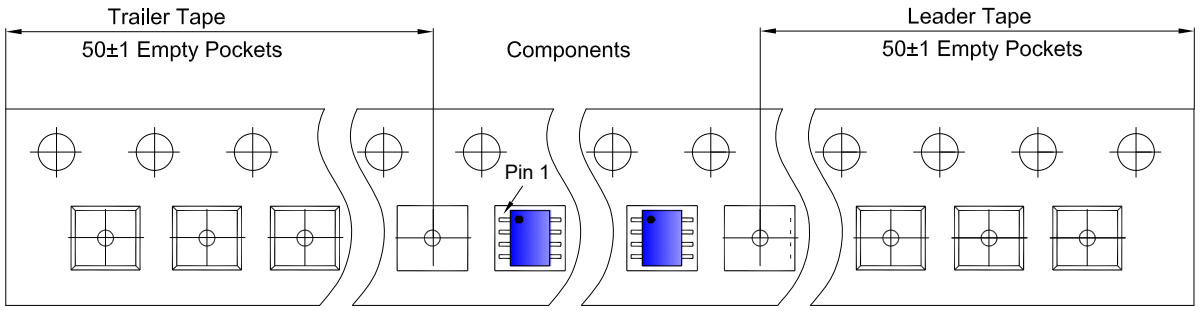
Packaging Description:

SOP8 parts are shipped in tape. The carrier tape is made from a dissipative (carbon filled) polycarbonate resin. The cover tape is a multilayer film (Heat Activated Adhesive in nature) primarily composed of polyester film, adhesive layer, sealant, and anti-static sprayed agent. These reeled parts in standard option are shipped with 2,500 units per 13" or 33cm diameter reel. The reels are clear in color and is made of polystyrene plastic (anti-static coated).

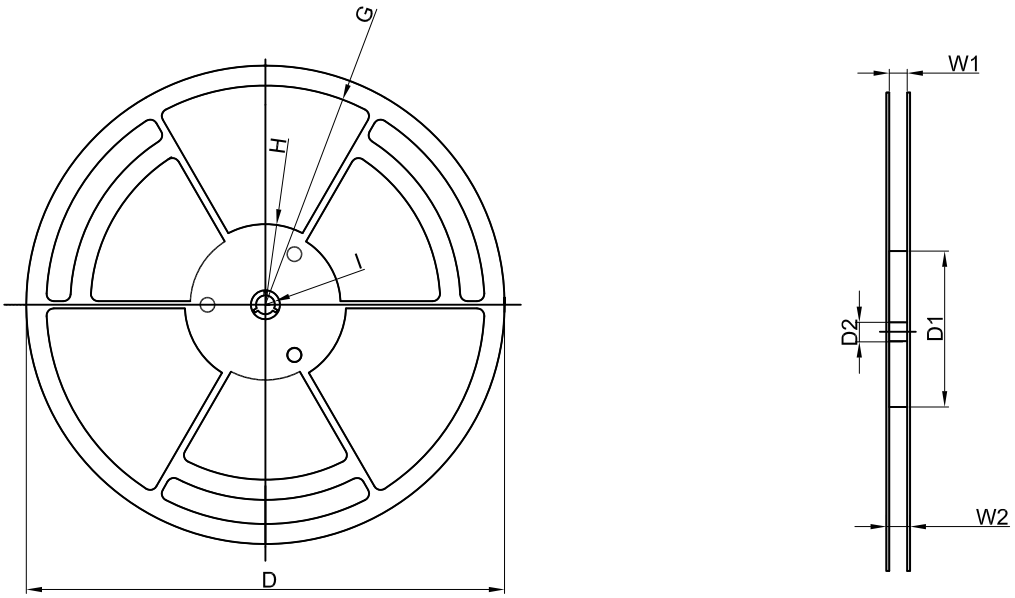
ALL DIM IN mm

Dimensions are in millimeter										
Pkg type	a	B	C	d	E	F	P0	P	P1	W
SOP8	6.40	5.40	2.10	Ø1.50	1.75	5.50	4.00	8.00	2.00	12.00

Tape Leader and Trailer



Reel



Dimensions are in millimeter								
Reel Option	D	D1	D2	G	H	I	W1	W2
13"Dia	Ø330.00	100.00	13.00	R151.00	R56.00	R6.50	12.40	17.60

REEL	Reel Size	Box	Box Size(mm)	Carton	Carton Size(mm)	G.W.(kg)
4,000 pcs	13 inch	8,000 pcs	360×360×65	64,000 pcs	565×380×390	

12 Notes and Revision History

12.1 Associated Product Family and Others

To view other products of the same type or IC products of other types, click the official website of SZCJ -- https: ***www.***szcjsemi.com for more details.

12.2 Notes

Electrostatic Discharge Caution



This IC may be damaged by ESD. Relevant personnel shall comply with correct installation and use specifications to avoid ESD damage to the IC. If appropriate measures are not taken to prevent ESD damage, the hazards caused by ESD include but are not limited to degradation of integrated circuit performance or complete damage of integrated circuit. For some precision integrated circuits, a very small parameter change may cause the whole device to be inconsistent with its published specifications.

12.3 Revision History

December 2024: released CJOA855x rev - 1.0.

DISCLAIMER

IMPORTANT NOTICE, PLEASE READ CAREFULLY

The information in this data sheet is intended to describe the operation and characteristics of our products. SZCJ has the right to make any modification, enhancement, improvement, correction or other changes to any content in this data sheet, including but not limited to specification parameters, circuit design and application information, without prior notice.

Any person who purchases or uses SZCJ products for design shall: 1. Select products suitable for circuit application and design; 2. Design, verify and test the rationality of circuit design; 3. Procedures to ensure that the design complies with relevant laws and regulations and the requirements of such laws and regulations. SZCJ makes no warranty or representation as to the accuracy or completeness of the information contained in this data sheet and assumes no responsibility for the application or use of any of the products described in this data sheet.

Without the written consent of SZCJ , this product shall not be used in occasions requiring high quality or high reliability, including but not limited to the following occasions: medical equipment, military facilities and aerospace. SZCJ shall not be responsible for casualties or property losses caused by abnormal use or application of this product.

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