SZCJ

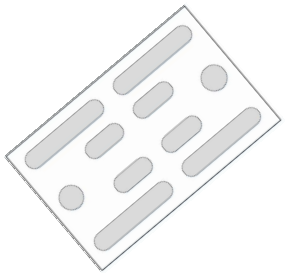
Shenzhen Changji Semiconductor Co., LTD.

CSP Enhancement Mode Power MOSFET

CJ25223SP-B Dual N-Channel MOSFET

V_{SSS}	$R_{SS(on)}$TYP	I_S
12V	2.3mΩ@4.5V	13.5A
	2.5mΩ@3.8V	
	3.0mΩ@3.1V	
	4.1mΩ@2.5V	

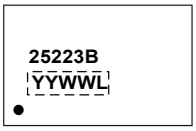
CSPC2115-10



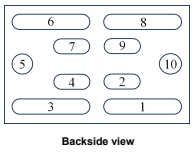
DESCRIPTION

The CJ25223SP-B uses advanced trench technology to provide excellent RSS(ON) , low gate charge and operation with gate voltages as low as 2.5V while retaining a 8V $V_{GS(MAX)}$ rating. It is ESD protected. This device is suitable for use as a unidirectional or bi-directional load switch, facilitated by its common-drain configuration.

Marking and pin assignment





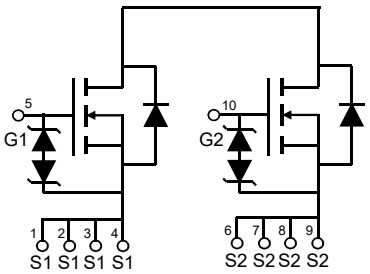


Marking:

1. 25223B: Product Code
2. YYWWL: Date Code
3. Solid dot: Pin 1

1,2,3,4 Source1
6,7,8,9 Source2
5 Gate1
10Gate2

Equivalent Circuit



ABSOLUTE MAXIMUM RATINGS (T_A=25℃ unless otherwise noted)

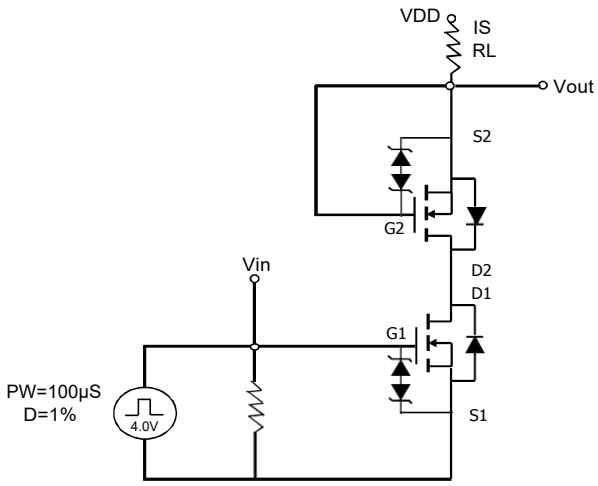
Parameter	Symbol	Limit	Unit
Source to Source Voltage	V_{SSS}	12	V
Gate-Source Voltage	V_{GSS}	±8	V
Source Current(DC)	I_S ①	13.5	A
Source Current (Pulsed)	I_{SP} ①②	135	A
Total Power Dissipation	P_T ①	0.58	W
Channel Temperature	T_{ch}	150	℃
Storage Temperature Range	T_{STG}	-55 To 150	℃

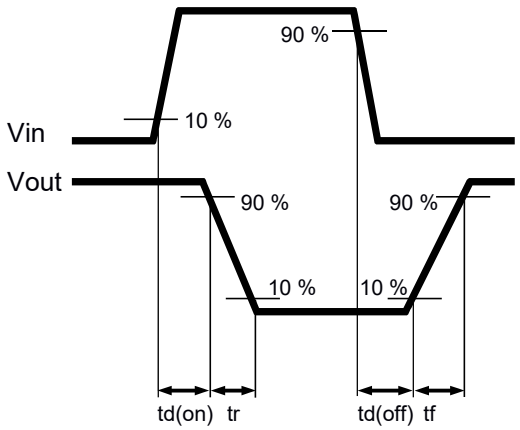
MOSFET ELECTRICAL CHARACTERISTICS

T_A=25℃ unless otherwise specified

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static Parameters						
Source to Source Breakdown Voltage	BV_{SSS}	I_S=1mA ,V_{GS}=0V	12			V
Zero-Gate Voltage Source Current	I_{SSS}	V_{SS}=12V,V_{GS}=0V			1.0	μA
Gate to Source Leakage Current	I_{GSS}	V_{SS}=0V, V_{GS}= ±8V			±10	μA
Gate to Source Threshold Voltage	$V_{GS(th)}$	V_{SS}=10V, I_S=250 μA	0.35	0.90	1.4	V
Source to Source On-state Resistance	$R_{SS(on)}$	V_{GS}=4.5V,I_S=2.0A	1.6	2.3	2.9	mΩ
		V_{GS}=3.8V,I_S=2.0A	1.7	2.5	3.2	mΩ
		V_{GS}=3.1V,I_S=2.0A	2.1	3.0	3.9	mΩ
		V_{GS}=2.5V,I_S=2.0A	2.8	4.1	5.8	mΩ
Input Capacitance	Ciss	V_{GS}=0V, V_{SS}=10V, f=1kHz		1680		pF
Output Capacitance	Coss			357		pF
Reverse Transfer Capacitance	Crss			306		pF
Turn-on Delay Time	$t_{d(on)}$ ③	V_{DD}=6V, R_L=1.5Ω, V_{GS}=4V		214		nS
Turn-on Rise Time	t_r ③			763		nS
Turn-off Delay Time	$t_{d(off)}$ ③			1.2		μS
Turn-off Fall Time	t_f ③			1.9		μS
Total Gate Charge	Q_g ③	V_{DD}=6V, V_{GS}=4V, I_D=10A		22		nC
Gate1-source1 charge	Q_{g1s1} ③			2.5		nC
Gate1-source2 charge	Q_{g1s2} ③			9.48		nC
Diode Forward Voltage	$V_{F(S-S)}$ ④	V_{GS}=0V,I_S=2A			1.0	V

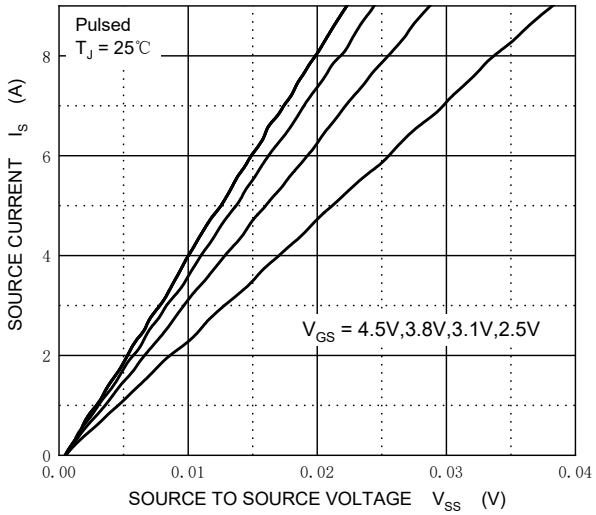
Notes: 1.Mounted on FR4 board (25.4mx25.4mmxt1.0mm) using minimum recommended pad size (partial coverage of single-sided 36um Copper).
2.t = 10 μs , Duty Cycle = 1 %.
3.When FET1 is measured,G2 and S2 are short-circuited.
4.When FET1 is measured,G2 and S2 are biased with V_{G2S2}=4.5V.



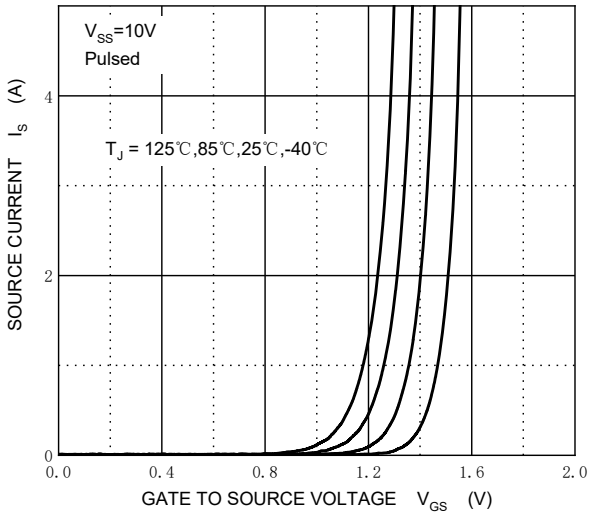


Typical Characteristics

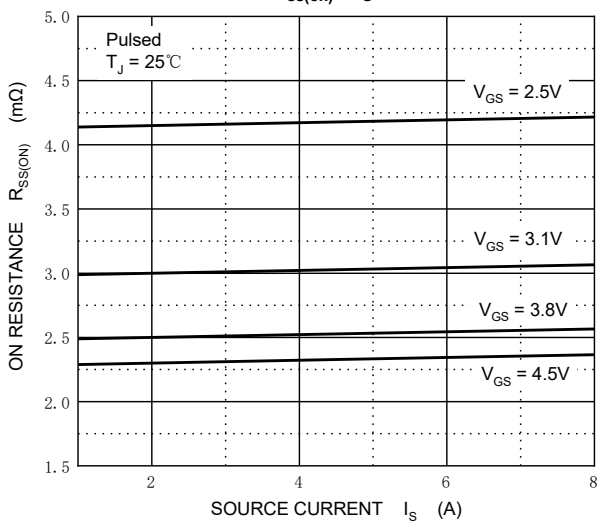
I_S—V_{SS}



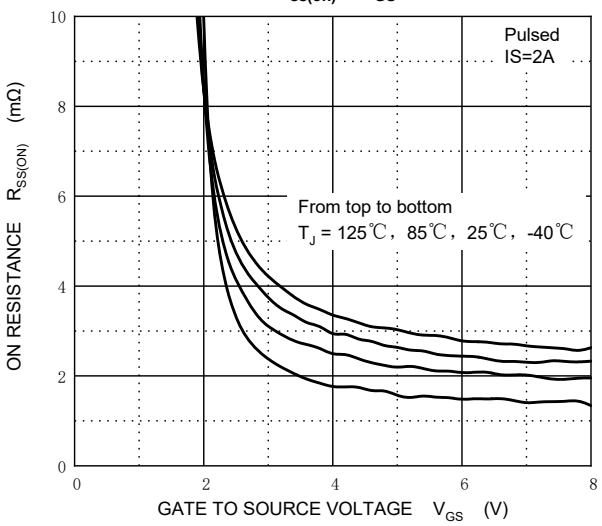
I_s—V_{GS}



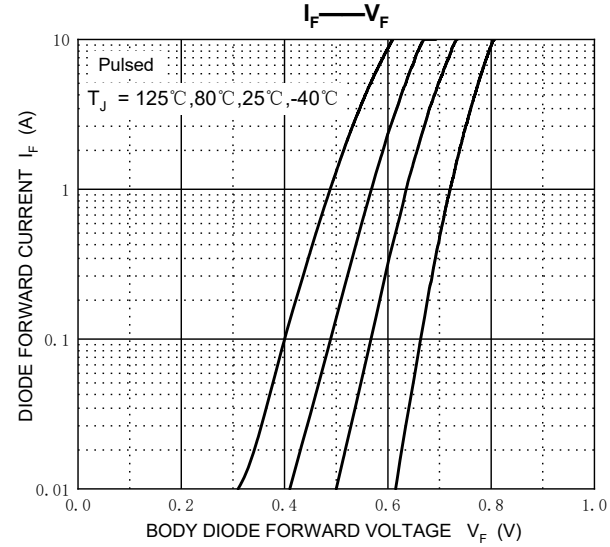
$R_{ss(on)}$—I_S



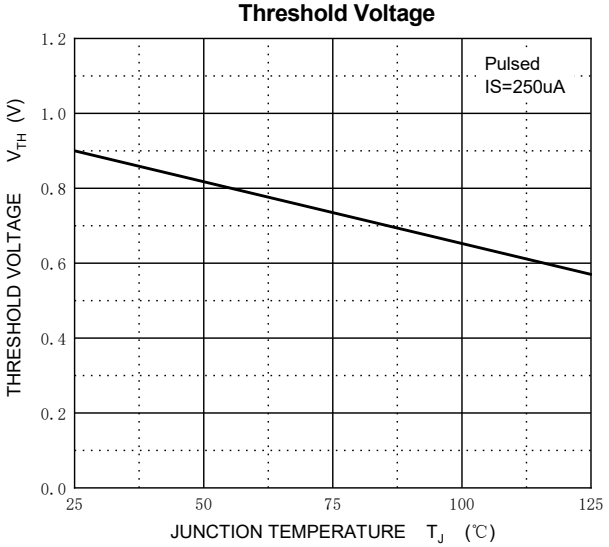
$R_{ss(on)}$—V_{GS}



I_F——V_F

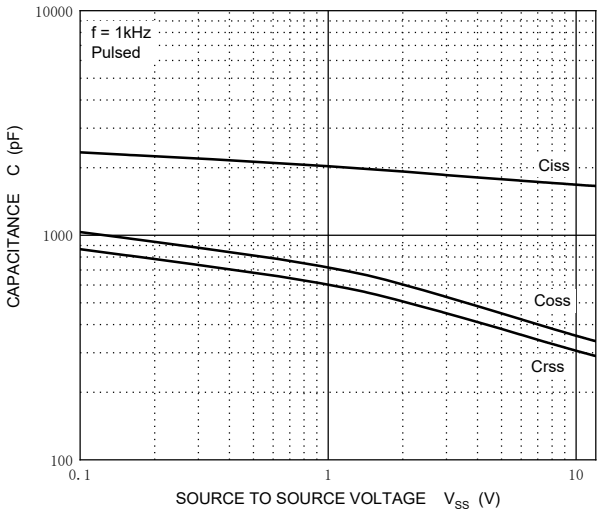


Threshold Voltage

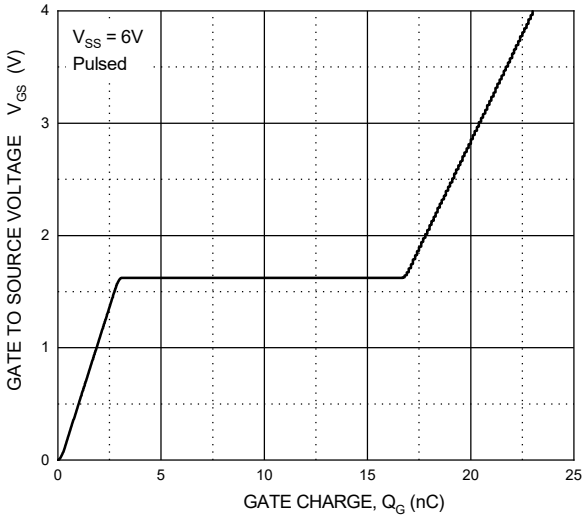


Typical Characteristics

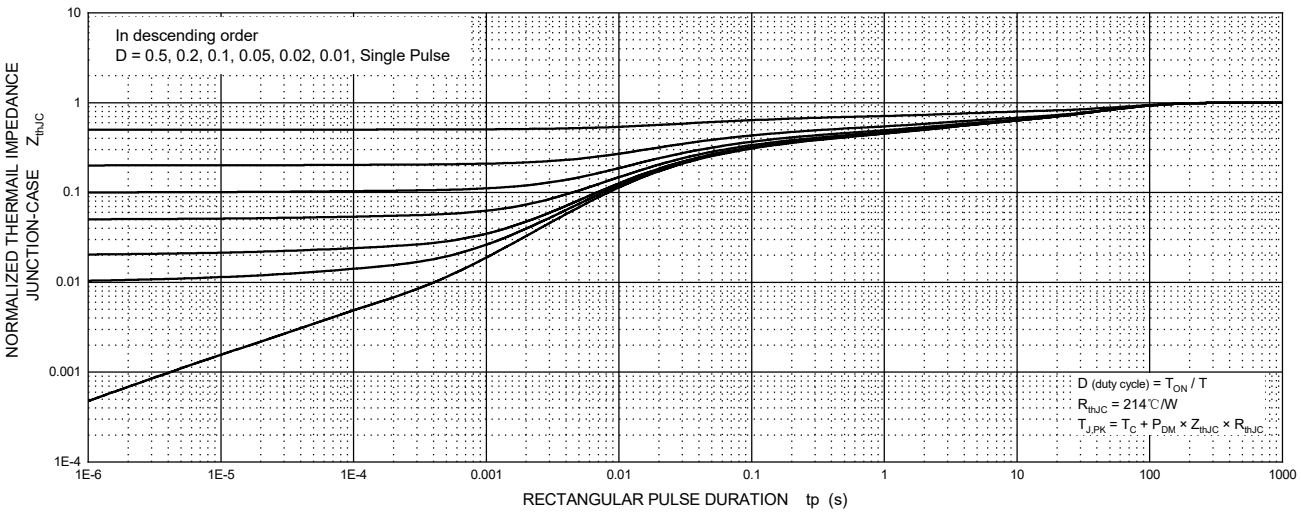
Capacitances



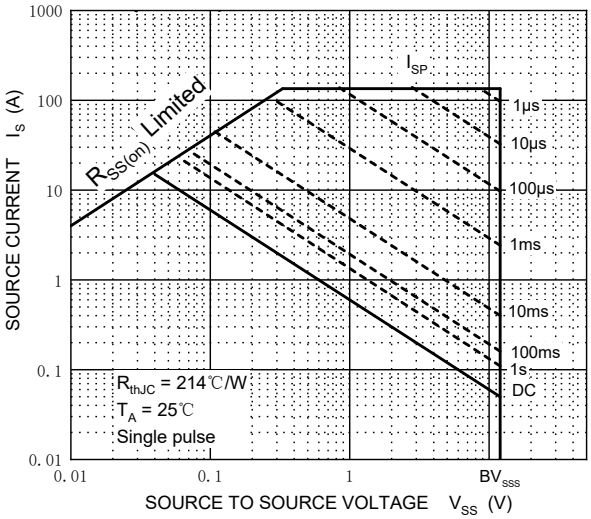
Gate Charge



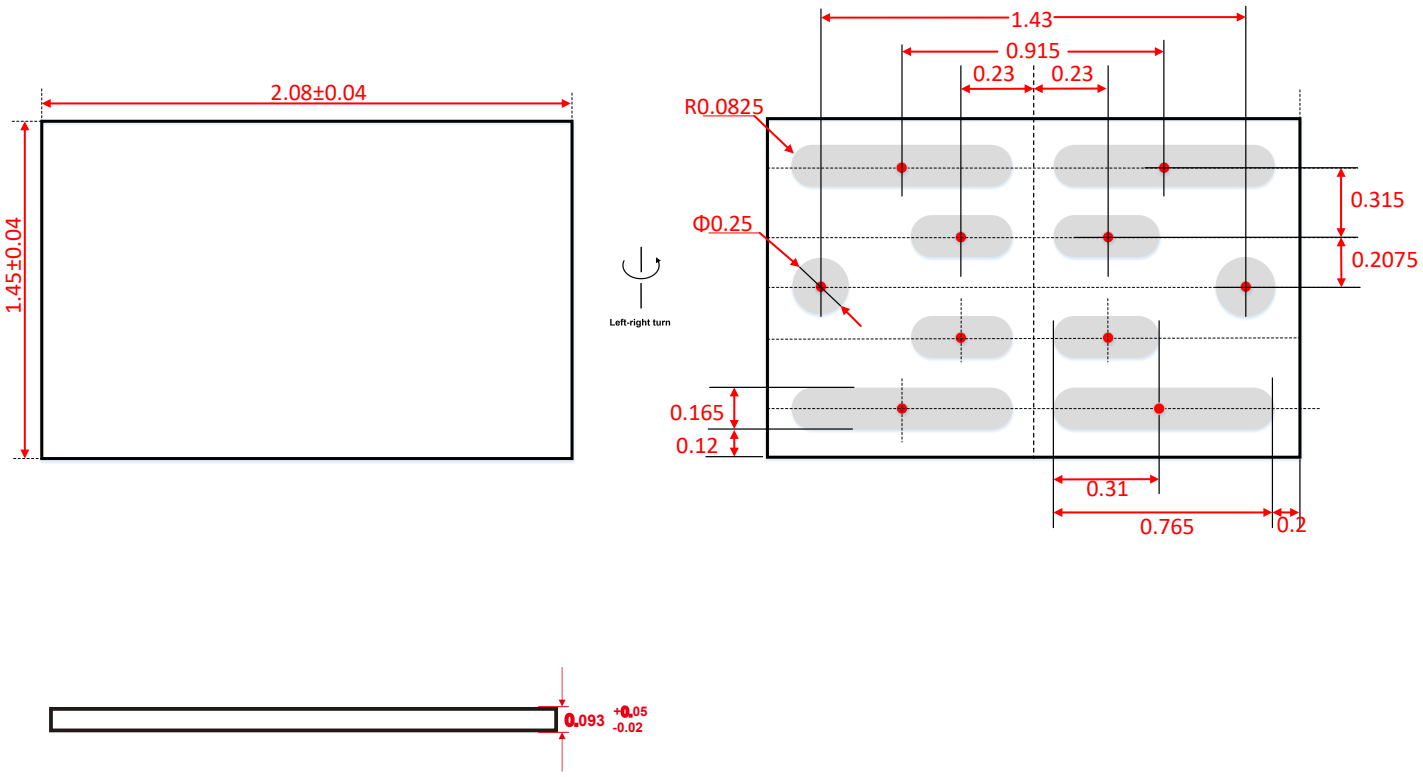
Transient Thermal Impedance, Junction-Case



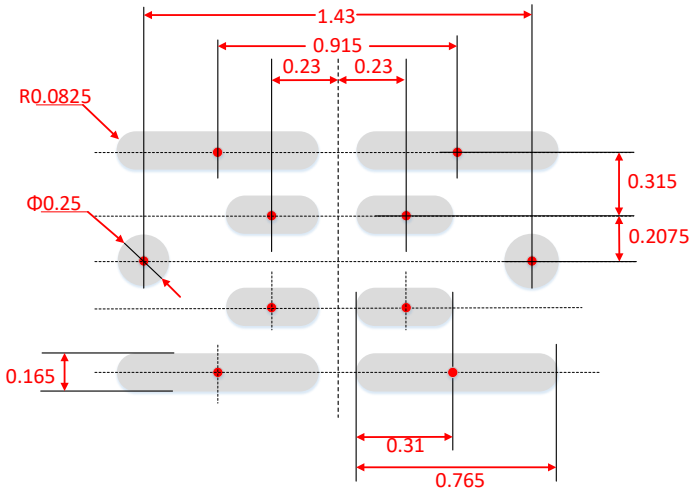
Maximum Safe Operating Area



CSPC2115-10 Package Outline Dimensions(Unit:mm)



CSPC2115-10 Suggested Pad Layout (Unit:mm)



Note:
1.Controlling dimension:in millimeters.
2.General tolerance:± 0.050mm.
3.The pad layout is for reference purposes only.

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