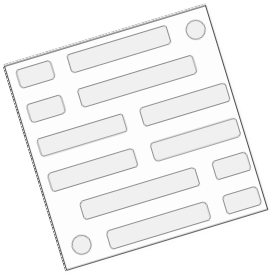
SZCJ Shenzhen Changji Semiconductor Co., LTD.

CSP Enhancement Mode Power MOSFET

CJ17133SP Dual N-Channel MOSFET

V_{SSS}	$R_{SS(on)}$TYP	I_S
24V	1.35mΩ@10V	16A
	1.50mΩ@8V	
	2.55mΩ@4.5V	

CSPC3030-14



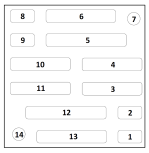
DESCRIPTION

The CJ17133SP uses advanced trench technology to provide excellent RSS(ON) , low gate charge and operation with gate voltages as low as 4.5V while retaining a 16V $V_{GS(MAX)}$ rating. It is ESD protected. This device is suitable for use as a unidirectional or bi-directional load switch, facilitated by its common-drain configuration.

Marking and pin assignment







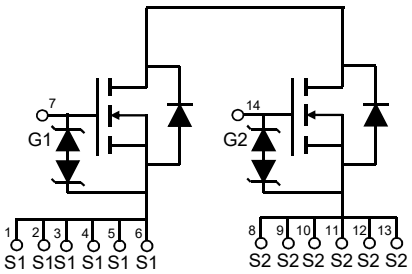
Backside view

Marking:

1. 17133: Product Code
2. YYMMS: Date Code
3. Solid dot: Pin 1

1,2,3,4,5,6 Source1
8,9,10,11,12,13 Source2
7 Gate1
14 Gate2

Equivalent Circuit



ABSOLUTE MAXIMUM RATINGS (T_A=25℃ unless otherwise noted)

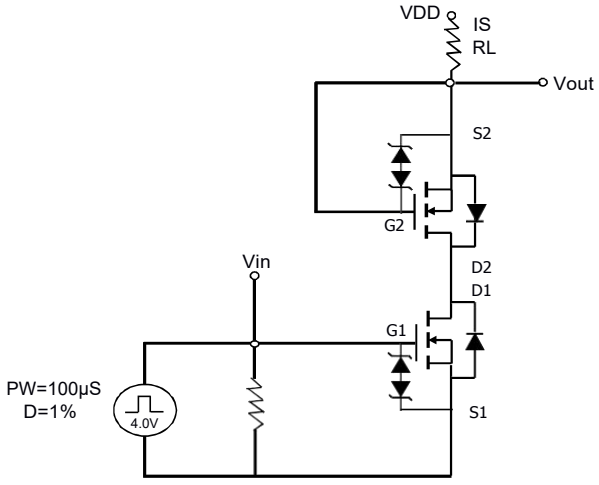
Parameter	Symbol	Limit	Unit
Source to Source Voltage	V_{SSS}	24	V
Gate-Source Voltage	V_{GSS}	±16	V
Source Current(DC)	I_S ①	16	A
Source Current (Pulsed)	I_{SP} ①②	160	A
Total Power Dissipation	P_T ①	1.3	W
Channel Temperature	T_{ch}	150	℃
Storage Temperature Range	T_{STG}	-55 To 150	℃

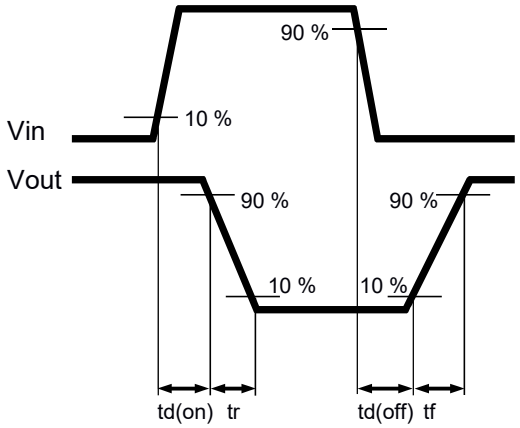
MOSFET ELECTRICAL CHARACTERISTICS

T_A=25℃ unless otherwise specified

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static Parameters						
Source to Source Breakdown Voltage	BV_{SSS}	I_S=1mA ,V_{GS}=0V	24			V
Zero-Gate Voltage Source Current	I_{SSS}	V_{SS}=24V,V_{GS}=0V			1.0	μA
Gate to Source Leakage Current	I_{GSS1}	V_{SS}=0V, V_{GS}= ±16V			±10	μA
	I_{GSS2}	V_{SS}=0V, V_{GS}= ±8V			1.0	μA
Gate to Source Threshold Voltage	$V_{GS(th)}$	V_{SS}=10V, I_S=1.34 mA	1	2	3	V
Source to Source On-state Resistance	$R_{SS(on)}$	V_{GS}=10V,I_S=2.0A	0.8	1.35	1.85	mΩ
		V_{GS}=8V,I_S=2.0A	0.9	1.50	2.35	mΩ
		V_{GS}=4.5V,I_S=2.0A	1.3	2.55	4.8	mΩ
Input Capacitance	Ciss	V_{GS}=0V, V_{SS}=10V, f=1kHz		3570		pF
Output Capacitance	Coss			720		pF
Reverse Transfer Capacitance	Crss			559		pF
Turn-on Delay Time	$t_{d(on)}$ ③	V_{DD}=12V, R_L=1.5Ω, V_{GS}=10V		215		nS
Turn-on Rise Time	t_r ③			330		nS
Turn-off Delay Time	$t_{d(off)}$ ③			1.5		μS
Turn-off Fall Time	t_f ③			1.1		μS
Total Gate Charge	Q_g ③	V_{DD}=12V, V_{GS}=10V, I_D=6A		67		nC
Gate1-source1 charge	Q_{g1s1} ③			10		nC
Gate1-source2 charge	Q_{g1s2} ③			20.6		nC
Diode Forward Voltage	$V_{F(S-S)}$ ④	V_{GS}=0V,I_S=2A			1.0	V

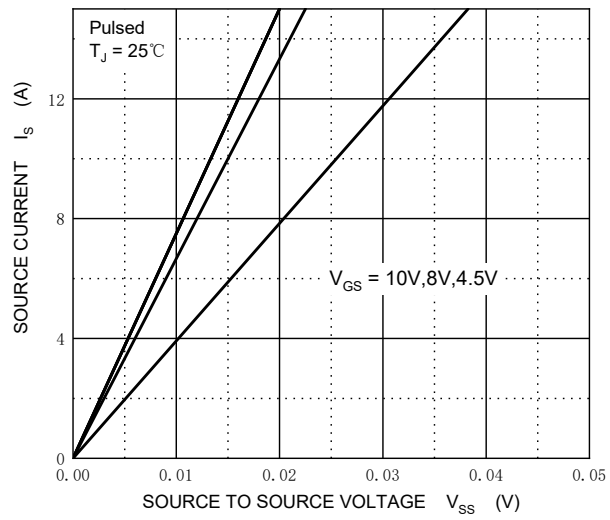
Notes: 1.Mounted on FR4 board (25.4mx25.4mmxt1.0mm) using minimum recommended pad size (partial coverage of single-sided 36um Copper).
2.t = 10 μs , Duty Cycle = 1 %.
3.When FET1 is measured,G2 and S2 are short-circuited.
4.When FET1 is measured,G2 and S2 are biased with V_{G2S2}=10V.



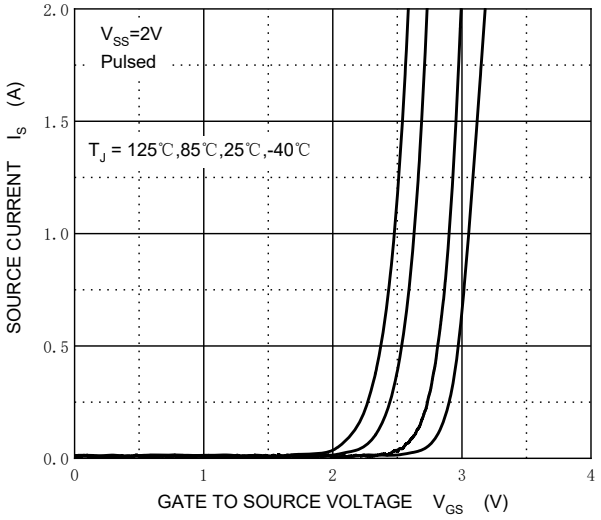


Typical Characteristics

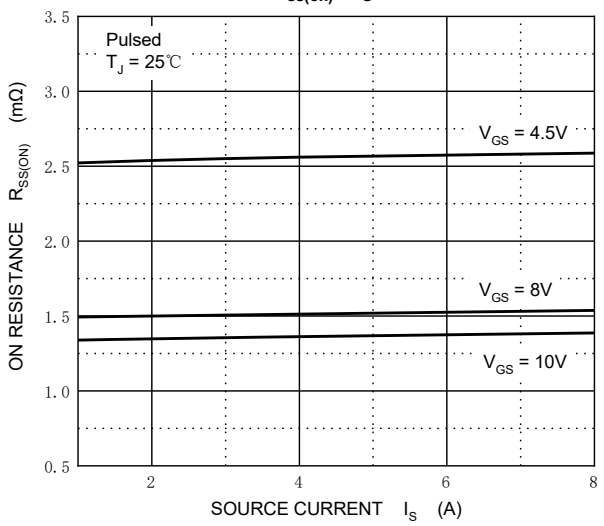
I_S—V_{SS}



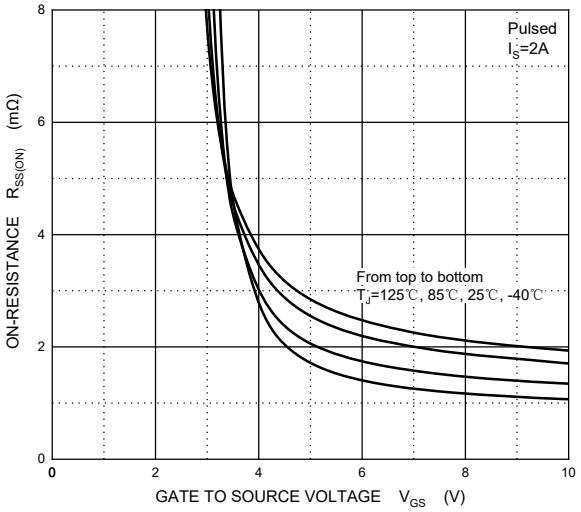
I_s—V_{GS}



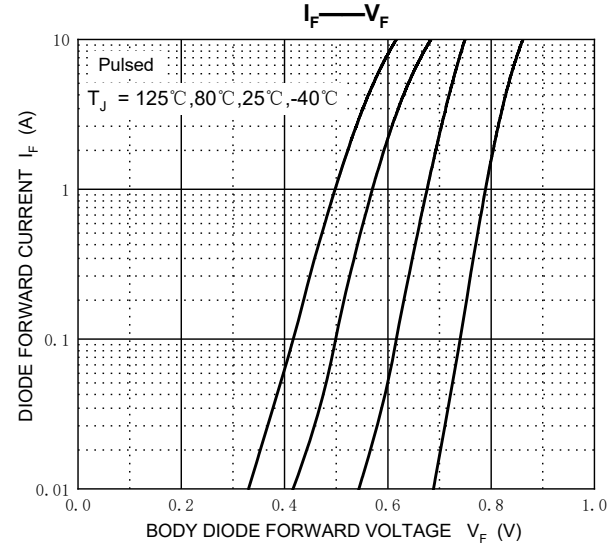
$R_{ss(on)}$—I_S



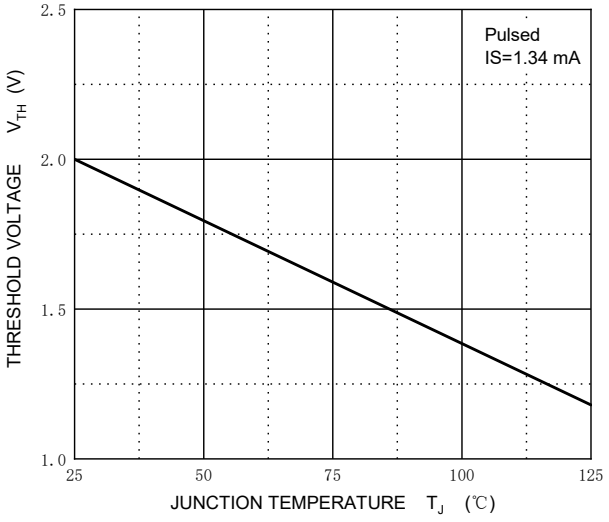
$R_{SS(ON)}$—V_{GS}



I_F——V_F

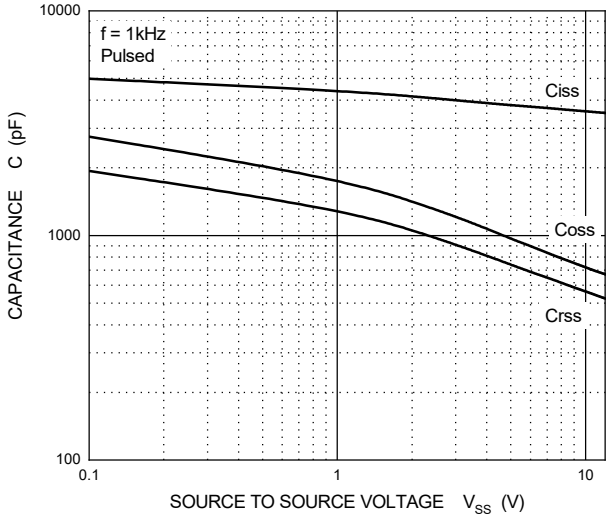


Threshold Voltage

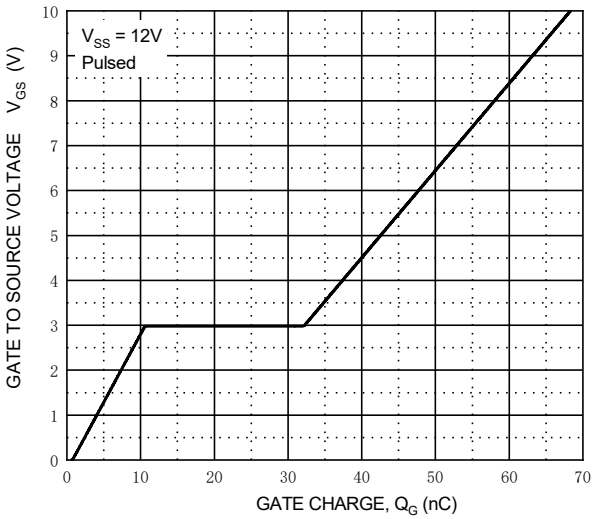


Typical Characteristics

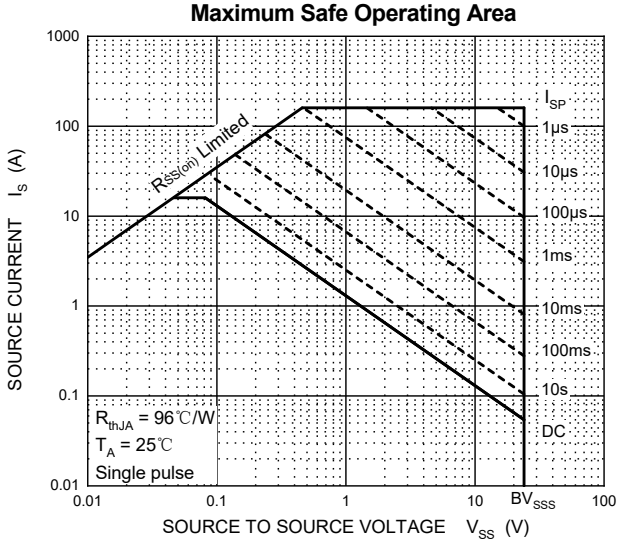
Capacitances



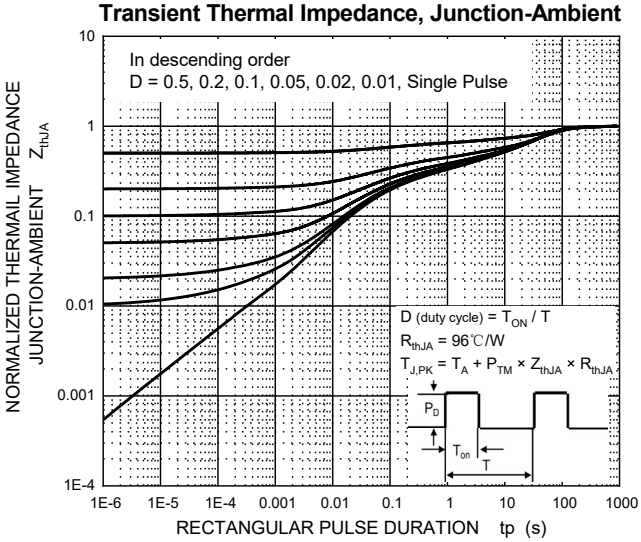
Gate Charge



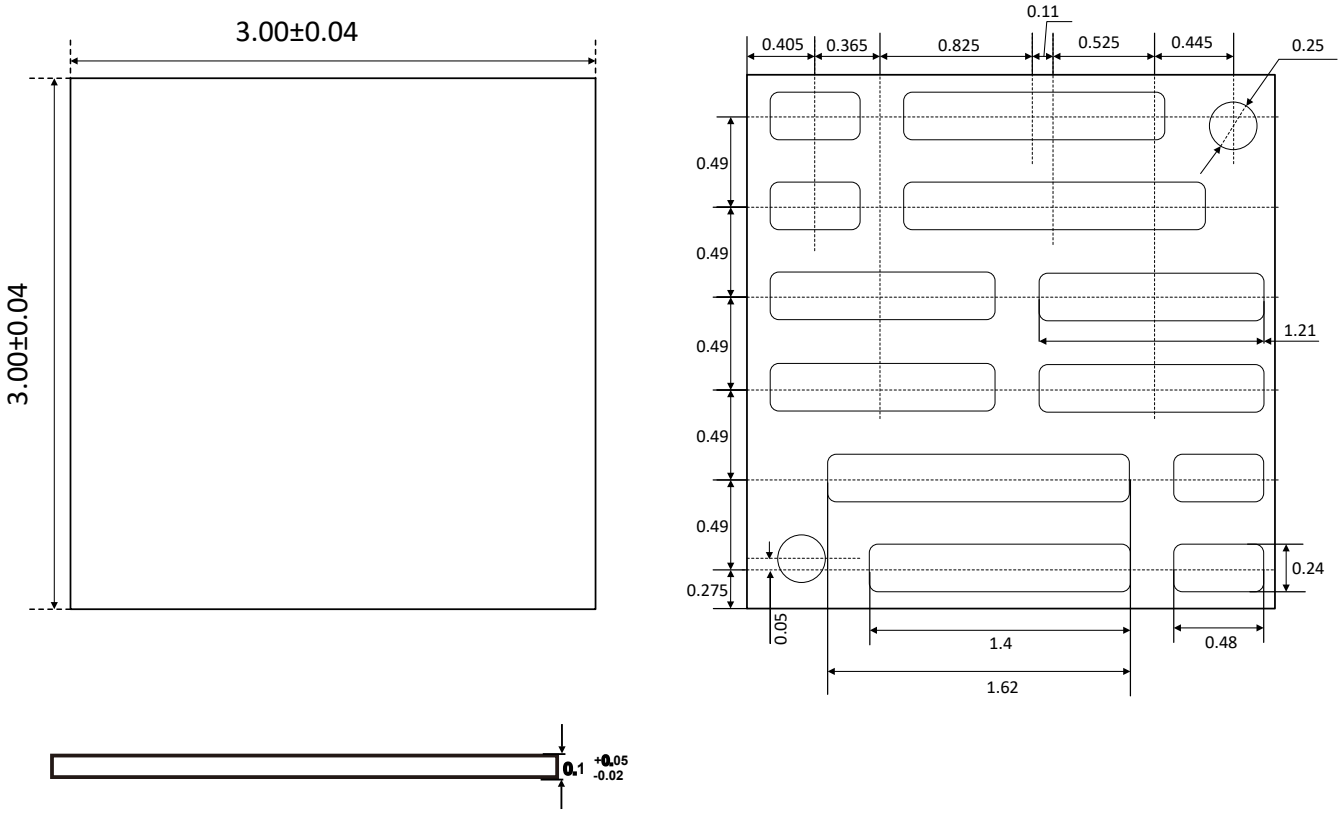
Maximum Safe Operating Area



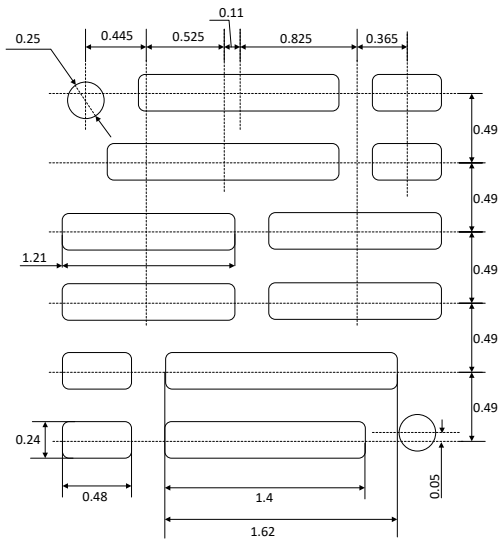
Transient Thermal Impedance, Junction-Ambient



CSPC3030-14 Package Outline Dimensions(Unit:mm)



CSPC3030-14 Suggested Pad Layout (Unit:mm)

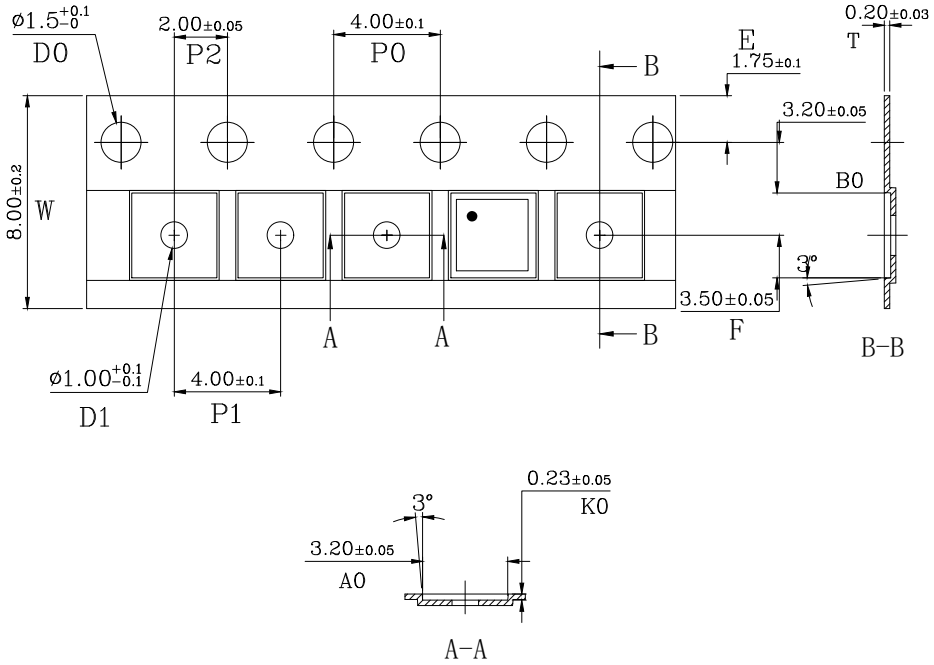


Note:
1.Controlling dimension:in millimeters.
2.General tolerance:± 0.050mm.
3.The pad layout is for reference purposes only.

NOTICE

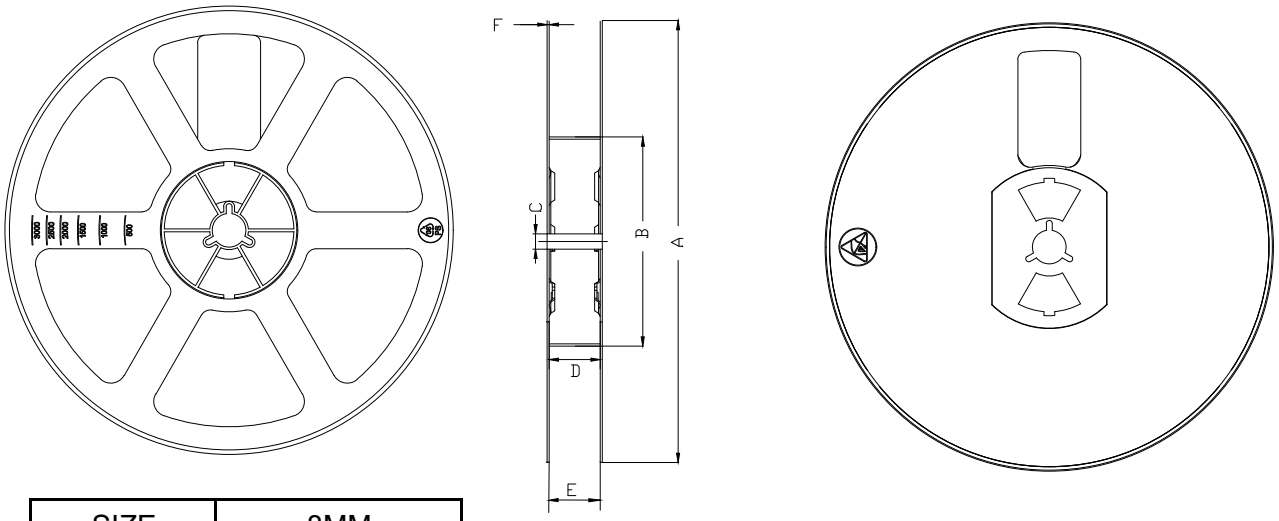
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Tape and Reel



产品尺寸规格(UNT:mm)

规格	W	P1	E	F	D0	D1
尺寸	8.00±0.20	4.00±0.10	1.75±0.10	3.50±0.05	1.50 +0.1 -0	1.00±0.10
规格	A0	B0	K0	T	P0	P2
尺寸	3.20±0.05	3.20±0.05	0.23±0.05	0.20±0.03	4.00±0.10	2.00±0.05



SIZE	8MM
A	178±2.0
B	55±1.0
C	13.0 +0.35 -0.15
D	8.4 +2.5 -0.4
E	8.65 +4.7 -0.65
F	1.5±0.5

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