4 ns, High Speed Comparator With Push-pull Outputs

CJCP61x Series Comparators

1 Introduction

The CJCP611/CJCP612/CJCP613 are single-, dual-channel comparators with push-pull output that feature 4ns propagation delay, a wide range of supply voltages from 2.7V to 5.5V with rail-to-rail inputs helps to implement in a wide variety of applications where require critical response time, power-sensitive, low-voltage. The output of the CJCP611/612/613 pulls to within 0.1V of either supply rail without external pull-up circuitry, making it ideal for interface with CMOS or TTL logic directly. All input and output pins can tolerate a continuous short-circuit fault condition to either rail. Internal hysteresis ensures clean output switching, even with slow-moving input signals.

The CJCP611 (single) is available in both SOT23-6L packages. The CJCP612 (dual) is offered in SOT23-8L, SOP8 and MSOP-8L packages, The CJCP613 (single) is offered in SOT23-5L and SOT-353 packages. All devices are rated over -40°C to +125°C extended industrial temperature range.

2 Features

- Fast 4ns Propagation Delay (100mV Overdrive)
- Rail-to-Rail I/O
- Shutdown version (CJCP611)
- Supply voltage: 2.7V to 5.5V
- Replacement for TLV3501, TLV3502
- Small packages: available in SOT23-5L, SOT-353, SOT23-6L, SOP8, SOT23-8L, MSOP-8L
- Low supply current: 3mA

3 Applications

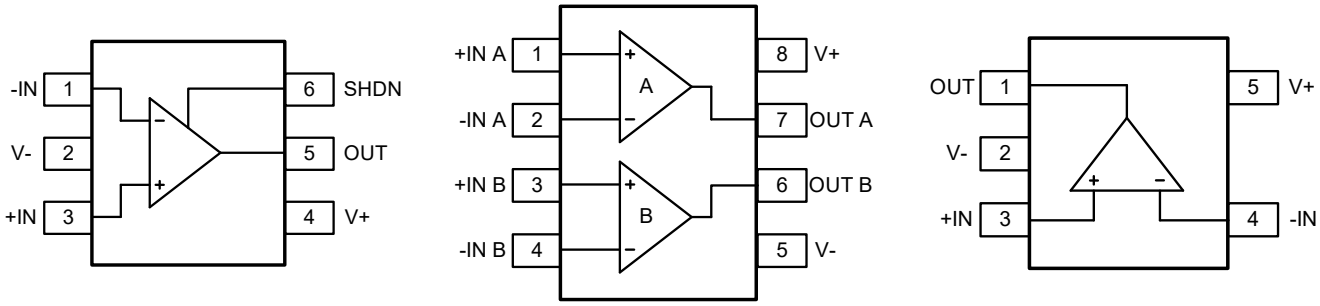
- High speed instrumentation
- Clock and data signal restoration
- Pulse spectroscopy
- High speed line receivers
- Threshold detection
- Peak and zero-crossing detectors
- High speed trigger circuitry
- Pulse-width modulators
- Current / voltage-controlled oscillators
- Automatic test equipment (ATE)
- Wireless Base Stations

4 Available Packages

PART NUMBER	PACKAGE
CJCP611-M6N	SOT-23-6L
CJCP612-M8N	SOT-23-8L
CJCP612-PAN	SOP8
CJCP612-PDN	MSOP8
CJCP613-M5N	SOT-23-5L
CJCP613-R5N	SOT-353

5 Pin Configuration and Marking Information

5.1 Pin Configuration and Function



CJCP611
SOT-23-6L

CJCP612
SOT-23-8L / SOP8 / MSOP8

CJCP613
SOT-23-5L / SOT-353

Figure 5-1. CJCP61x Pin Map

Pin Function: CJCP611

PIN NAME	PIN NUMBER	I / O	DESCRIPTION
-IN	1	I	Negative (Inverting) input
V-	2	-	Negative (lowest) power supply
+IN	3	I	Positive (noninverting) input
V+	4	-	Positive (highest) power supply
OUT	5	O	Output
SHDN	6	I	Shutdown (the device is idle when this pin is not in use)

Pin Function: CJCP612

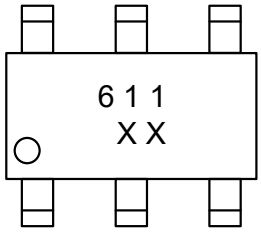
PIN NAME	PIN NUMBER	I / O	DESCRIPTION
+IN A	1	I	Noninverting input, channel A
-IN A	2	I	Inverting input, channel A
+IN B	3	I	Noninverting input, channel B
-IN B	4	I	Inverting input, channel B
V-	5	-	Negative (lowest) power supply
OUT B	6	O	Output, channel B
OUT A	7	O	Output, channel A
V+	8	-	Positive (highest) power supply

Pin Function: CJCP613

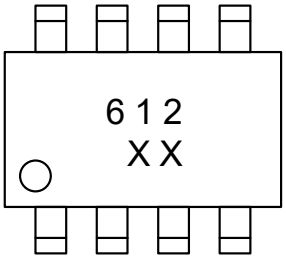
PIN NAME	PIN NUMBER	I / O	DESCRIPTION
OUT	1	O	Output
V-	2	-	Negative (lowest) power supply
+IN	3	I	Positive (noninverting) input
-IN	4	I	Negative (Inverting) input
V+	5	-	Positive (highest) power supply

5 Pin Configuration and Marking Information

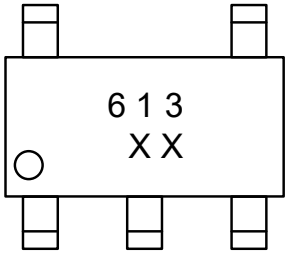
5.2 Marking Information



SOT-23-6L



SOT-23-8L / SOP8 / MSOP8



SOT-23-5L / SOT-353

"**61x**": Device number.

"**XX**": Code, indicates weekly record information.

6 Specifications

6.1 Absolute Maximum Ratings

over operating ambient temperature range, unless otherwise specified(1).

CHARACTERISTIC		SYMBOL	VALUE	UNIT
Supply voltage[(V+) - (V-)]		V_S	6	V
Signal input pins	Voltage(2)		(V-) - 0.3V ~ (V+) + 0.3V	V
	Current(2)		±10	mA
Output short-circuit			Continuous(3)	mA
Maximum junction temperature		$T_{J\ MAX}$	150	°C
Storage temperature		T_{stg}	-65 ~ +150	°C
Soldering temperature & time		T_{solder}	260°C, 10s	-

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum rated conditions for extended periods may affect device reliability.

(2) Input pins are diode-clamped to the power-supply rails. Current limit input signals that can swing more than 0.5V beyond the supply rails to 10mA or less.

(3) Short circuits from outputs to V_S can cause excessive heating and eventual destruction. A heat sink may be required to keep the junction temperature below the absolute maximum. This depends on the power supply voltage and how many amplifiers are shorted. Thermal resistance varies with the amount of PC board metal connected to the package. The specified values are for short traces connected to the leads.

6.2 Recommend Operating Conditions

over operating ambient temperature range, unless otherwise specified.

PARAMETER	SYMBOL	MIN.	NOM.	MAX.	UNIT
Power supply range	V_S	2.7		5.5	V
Operating ambient temperature	T_A	-40		+125	°C

6 Specifications

6.3 ESD Ratings

ESD RATINGS		VALUE	UNIT
Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(4)	5000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(5)	2000	V
	Machine model (MM), per JESD22-A115C	250	V

(4) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

(5) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.4 Thermal Information

THERMAL METRIC(6)	SYMBOL	SOT-23-5L	SOT-23-6L	SOT-23-8L	SOT-353	SOP8	MSOP8	UNIT
Junction-to-ambient thermal resistance	$R_{\Theta JA}$	250.0	240.0	189.4	260.0	165.0	201.6	°C/W
Reference maximum power dissipation (continuous)	$P_{D\ Ref}$	0.40	0.42	0.53	0.38	0.61	0.62	W

(6) T_A = 25°C, measured on evaluation board with 1oz. copper traces of minimum pad size, all device outputs were active.

6 Specifications

6.5 Electrical Characteristics

V_S = (V+) - (V-) = 5.0V, T_A = 25°C, unless otherwise noted.

Boldface limits apply over the specified temperature range, T_A = -40°C to +125°C.

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
OFFSET VOLTAGE						
Input offset voltage	V_{OS}	V_{CM} = 0V, I_O = 0mA		2		mV
Offset voltage drift	V_{OS} TC	T_A = -40°C to +125°C		2		µV/°C
Power supply rejection ratio	PSRR	V_S = 2.7 to 5.5V		500		µV/V
Input hysteresis				10		mV
INPUT VOLTAGE RANGE						
Common-mode voltage range	V_{CM}		(V-) − 0.1		(V+) + 0.1	V
Common-mode rejection ratio	CMRR	V_{CM} = -0.2 to (V+) + 0.2V		60		dB
		V_{CM} = -0.2 to (V+) + 0.2V, T_A = -40°C to +125°C		58		
OUTPUT						
Voltage output swing from rail	V_{OH}, V_{OL}	I_{OUT} = ±1mA		20	50	mV
SHUTDOWN (CJCP611 only)						
Shutdown turn off time	t_{OFF}			55		ns
Shutdown turn on time	t_{ON}			60		ns
SHDN low threshold	V_L	Comparator is enabled			(V+) – 1.7	V
SHDN high threshold	V_H	Comparator is disabled	(V+) – 0.9			V
Quiescent current in shutdown	I_{QSD}			6		µA
POWER SUPPLY						
Quiescent current	I_Q	V_S = 5V, V_O = High		3	6	mA

V_S = (V+) - (V-) = 5.0V, T_A = 25°C, unless otherwise noted.

Boldface limits apply over the specified temperature range, T_A = -40°C to +125°C.

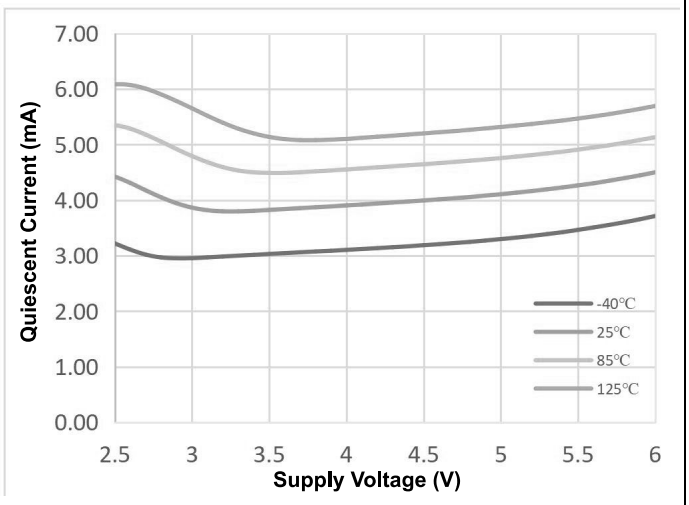
CHARACTERISTIC	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Propagation delay time	$T_{(pd)}$	V_{dd} = 5.5V Input Overdrive = 20mV	T_A = 25°C		6		ns
			T_A = -40°C to +125°C		7		ns
		V_{dd} = 5.5V Input Overdrive = 100mV	T_A = 25°C		4		ns
			T_A = -40°C to +125°C		5		ns
Rise time	t_R	Measured between 10% to 90% of V_S			1		ns
Fall time	t_F	Measured between 90% to 10% of V_S			1		ns

6 Specifications

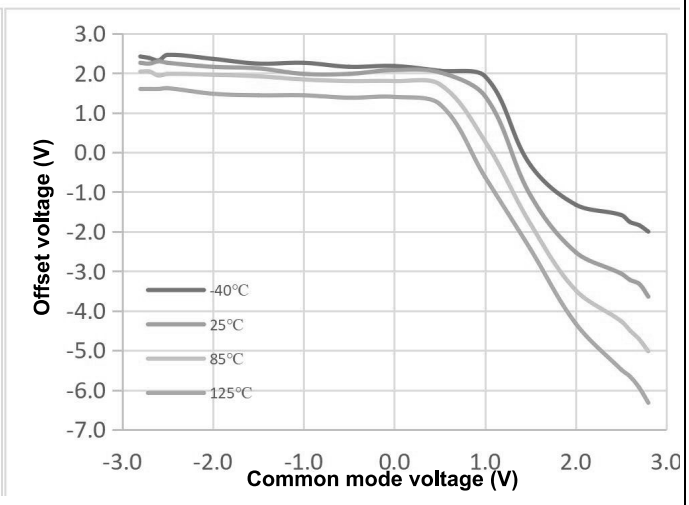
6.6 Typical Characteristics

V_S = (V+) - (V-) = 5.0V, T_A = 25°C, unless otherwise noted.

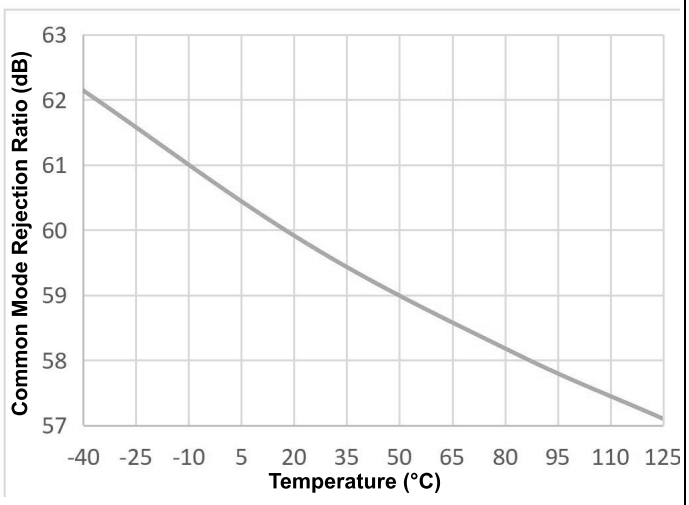
Quiescent Current vs Supply Voltage Voltage



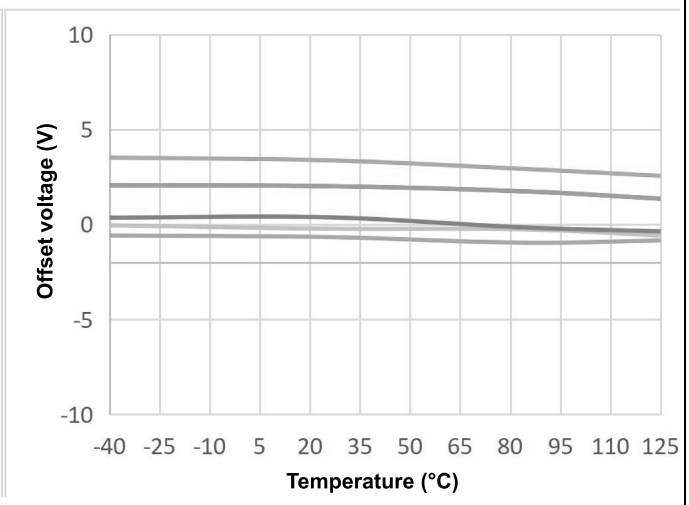
Offset Voltage vs Common mode Voltage



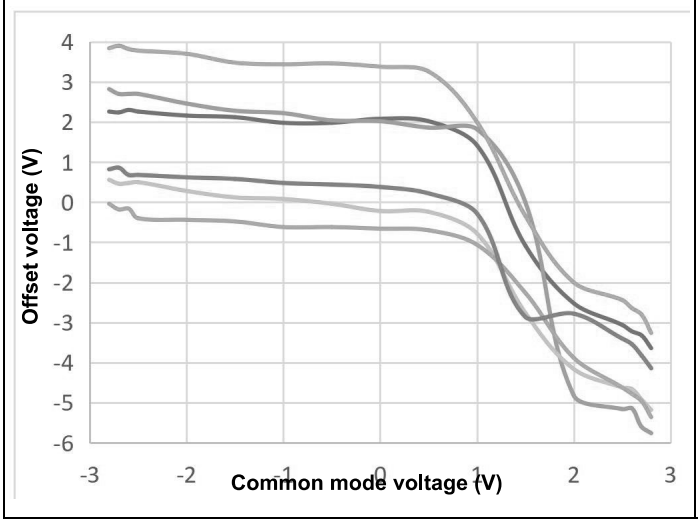
Common mode rejection ratio vs Temperature



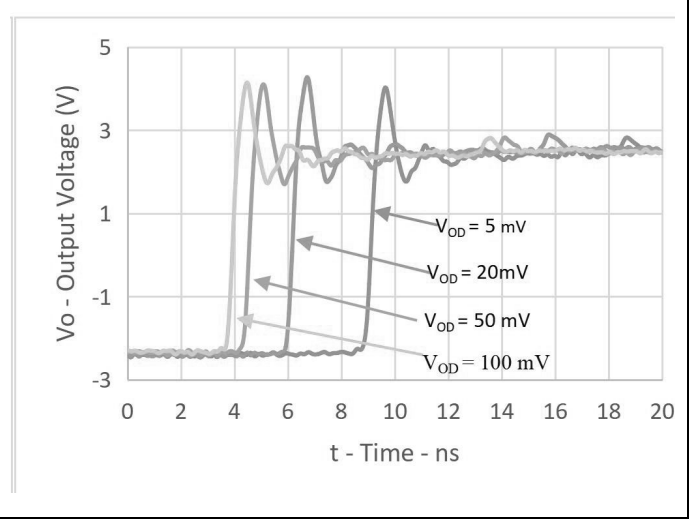
Offset Voltage vs Temperature



Offset Voltage vs Common mode Voltage



Propagation Delay Rising Edge

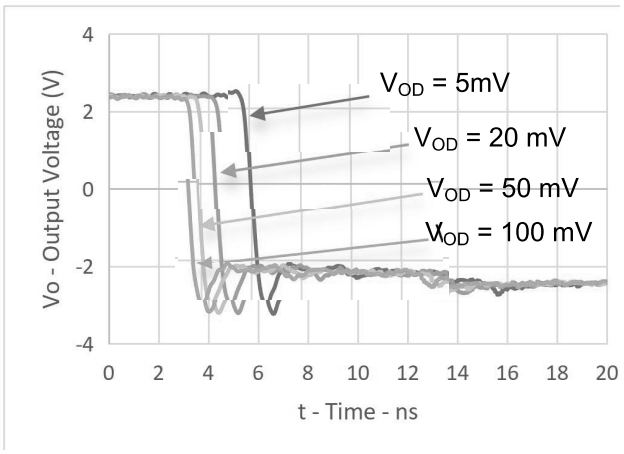


6 Specifications

6.6 Typical Characteristics(continue)

V_S = (V+) - (V-) = 5.0V, T_A = 25°C, unless otherwise noted.

Propagation Delay Falling Edge



7 Detail Description

Operating Voltage

The CJCP61x family of micro-power push pull output comparators is fully specified and ensured for operation from 2.7 to 5.5V and offers an excellent speed-to-power combination with propagation delay of 4ns and a quiescent supply current of 3mA.This combination of fast response time at micro-power enables power conscious systems to monitor and respond quickly to fault conditions.

In addition, and many specifications apply over the industrial temperature range of -40°C to +85°C, parameters that vary significantly with operating voltages or temperature are illustrated in the Typical Characteristics graphs.

Shutdown

A shutdown pin (CJCP611 only) allows the device to go into idle when it is not in use. When the shutdown pin is high, the device draws approximately TBD μA, and the output goes to high impedance. When the shutdown pin is low, the CJCP611 is active. When the CJCP611 shutdown feature is not used, connect the shutdown pin to the most negative supply, as shown in Figure 10. Exiting shutdown mode requires approximately TBD ns. The CJCP612 and CJCP613 do not have the shutdown feature.

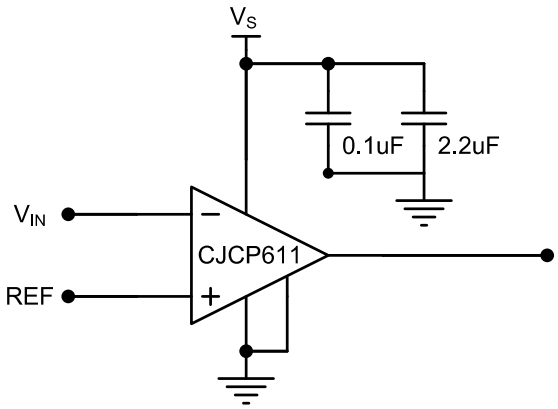


Figure 10: Basic connections for the CJCP611

Input Voltage

The CJCP611/612/613 comparator family uses CMOS transistors at the inputs which prevent phase inversion when the input pins exceed the supply voltages.

Internal ESD protection diodes (D1，D2，D3，and D4) that are connected between the inputs and each supply rail. These diodes protect the input transistors in the event of electrostatic discharge and are reverse biased during normal operation. This protection scheme allows voltages as high as approximately 300mV beyond the rails to be applied at the input of either terminal without causing permanent damage. See the table of Absolute Maximum Ratings for more information.

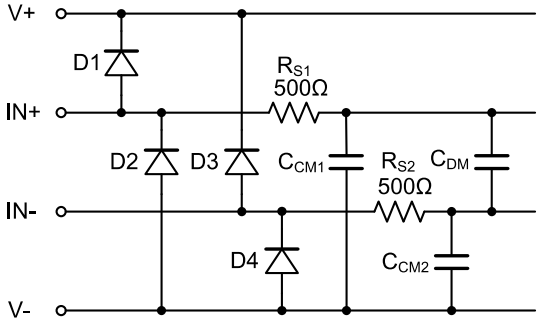


Figure 11: Input EMI Filter and Clamp Circuit

7 Detail Description (continued)

EMI Rejection Ratio

Circuit performance is often adversely affected by high frequency EMI. When the signal strength is low and transmission lines are long, an op-amp must accurately amplify the input signals. However, all op-amp pins — the non-inverting input, inverting input, positive supply, negative supply, and output pins — are susceptible to EMI signals. These high frequency signals are coupled into an op-amp by various means, such as conduction, near field radiation, or far field radiation. For example, wires and printed circuit board (PCB) traces can act as antennas and pick up high frequency EMI signals.

Amplifiers do not amplify EMI or RF signals due to their relatively low bandwidth. However, due to the nonlinearities of the input devices, op-amps can rectify these out of band signals. When these high frequency signals are rectified, they appear as a dc offset at the output.

The CJCP61x op-amps have integrated EMI filters at their input stage. A mathematical method of measuring EMIRR is defined as follows:

$$EMIRR = 20 \log (V_{IN_PEAK} / \Delta_{VOS})$$

Internal Hysteresis

Most high-speed comparators oscillate in the linear region because of noise or undesired parasitic feedback. This tends to occur when the voltage on one input is at or equal to the voltage on the other input. To counter the parasitic effects and noise, the devices have an internal hysteresis of 5mV.

The hysteresis in a comparator creates two trip points: one for the rising input voltage and one for the falling input voltage. The difference between the trip points is the hysteresis. The average of the trip points is the offset voltage. When the comparator's input voltages are equal, the hysteresis effectively causes one comparator input voltage to move quickly past the other, thus taking the input out of the region where oscillation occurs. Standard comparators require hysteresis to be added with external resistors. Figure 12 illustrates the case where IN- is fixed and IN+ is varied. If the inputs were reversed, the figure would look the same, except the output would be inverted.

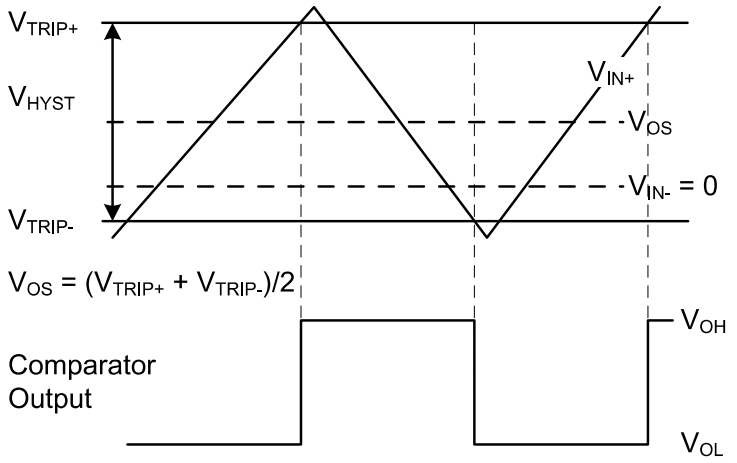


Figure 12: Input and Output waveform, Non-inverting input varied

Maximizing performance through proper layout

To achieve the maximum performance of the extremely high input impedance and low offset voltage of the CJCP611/ CJCP612/CJCP613 devices，care is needed in laying out the circuit board. The PCB surface must remain clean and free of moisture to avoid leakage currents between adjacent traces. Surface coating of the circuit board reduces surface moisture and provides a humidity barrier，reducing parasitic resistance on the board. The use of guard rings around the comparator inputs further reduces leakage currents. Figure 13 shows proper guard ring configuration and the top view of a surface-mount layout. The guard ring does not need to be a specific width, but it should form a continuous loop around both inputs. By setting the guard ring voltage equal to the voltage at the

7 Detail Description (continued)

non-inverting input, parasitic capacitance is minimized as well. For further reduction of leakage currents, components can be mounted to the PCB using Teflon standoff insulators.

Other potential sources of offset error are thermo-electric voltages on the circuit board. This voltage, also called Seebeck voltage, occurs at the junction of two dissimilar metals and is proportional to the temperature of the junction. The most common metallic junctions on a circuit board are solder-to-board trace and solder-to-component lead. If the temperature of the PCB at one end of the component is different from the temperature at the other end, the resulting Seebeck voltages are not equal, resulting in a thermal voltage error. This thermocouple error can be reduced by using dummy components to match the thermoelectric error source. Placing the dummy component as close as possible to its partner ensures both Seebeck voltages are equal, thus canceling the thermocouple error. Maintaining a constant ambient temperature on the circuit board further reduces this error. The use of a ground plane helps distribute heat throughout the board and reduces EMI noise pickup.

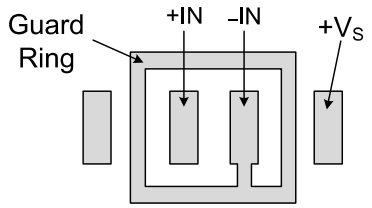


Figure 13. Use a guard ring around sensitive pins

Input and Output coupling

To minimize capacitive coupling, the input and output signal traces should not be parallel. This helps reduce unwanted positive feedback.

8 Application and Implementation

8.1 Typical Application Circuits

Inverting External Hysteresis

The CJCP61x has robust performance when used with a good layout. However, the comparator input has almost no immunity in the range of a specific offset voltage (±5mV). For slow moving or noisy input signals When the input signal moves past the switching threshold, the comparator output may cause an unwanted switching state. In such applications, the CJCP61x's 10mV internal hysteresis may not be sufficient. To increase hysteresis and noise margin even more, add positive feedback with two resistors as a voltage divider from the output to the non-inverting input.

Figure 14 shows a typical topology used to introduce additional hysteresis.

Figure 15 shows equivalent circuit when V_{OUT} switch from low to high.

Figure 16 shows equivalent circuit when V_{OUT} switch from high to low.

Use equation 1 to calculate Vtr (The voltage which let output switch from low to high) and use equation 2 to calculate Vtf (The voltage which let output switch from high to low). Finally the approximate total hysteresis could be calculated by using equation 3.

$$V_{tr} = (V_{CC} - V_{ref}) \times R2 / (R1 + R2) + V_{ref} \quad (1)$$

$$V_{tf} = R1 \times V_{ref} / (R1 + R2) \quad (2)$$

$$V_{HYST} = (V_{tr} - V_{tf}) + V_{HYST\text{-}INTL} = (V+) \times 2 / (R1 + R2) + 10mV \quad (3)$$

The total hysteresis, V_{HYST}, sets the value of the transition voltage required to switch the comparator output, by enlarging the threshold region, thereby reducing sensitivity to noise.

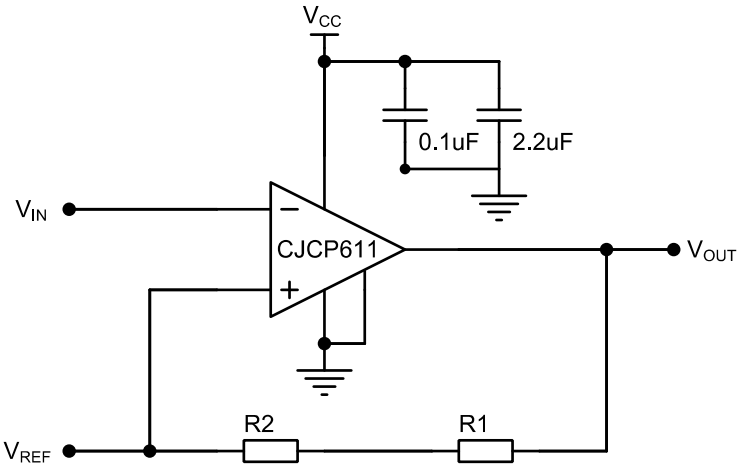


Figure 14: Adding External Hysteresis of CJCP61x

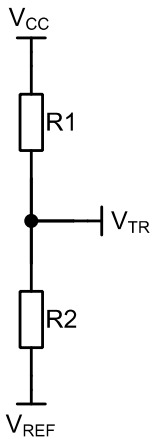


Figure 15: Equivalent circuit – Vout from low to high

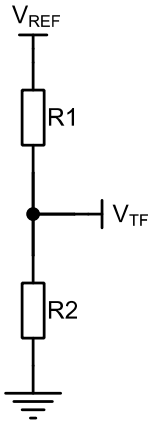


Figure 16: Equivalent circuit – Vout from high to low

8 Application and Implementation

8.1 Typical Application Circuits (continue)

Non-Inverting External Hysteresis

A non-inverting comparator with hysteresis requires a two-resistor network, as shown in Figure 17, and a voltage reference (V_{REF}) at the inverting input. When V_{IN} is low, the output is also low. For the output to switch from low to high, V_{IN} must rise up to V_{tr}. V_{tr} is calculated by Equation 5.

$V_{ref} = R2 / (R1 + R2) \times V_{CC}$ (4)

$V_{tr} = V_{ref} / R3 \times (R3 + R4)$ (5)

When V_{IN} is high, the output is also high. In order for the comparator to switch back to a low state, V_{IN} can be calculated by Equation 6. Finally the approximate total hysteresis could be calculated by using equation 7.

$V_{tf} = (V_{ref} \times (R3 + R4) – V_{CC} \times R4) / R3$ (6)

$V_{HYST} = (V_{tr} - V_{tf}) + V_{HYST-INTL} = R4 / R3 \times V_{CC} + 10mV$ (7)

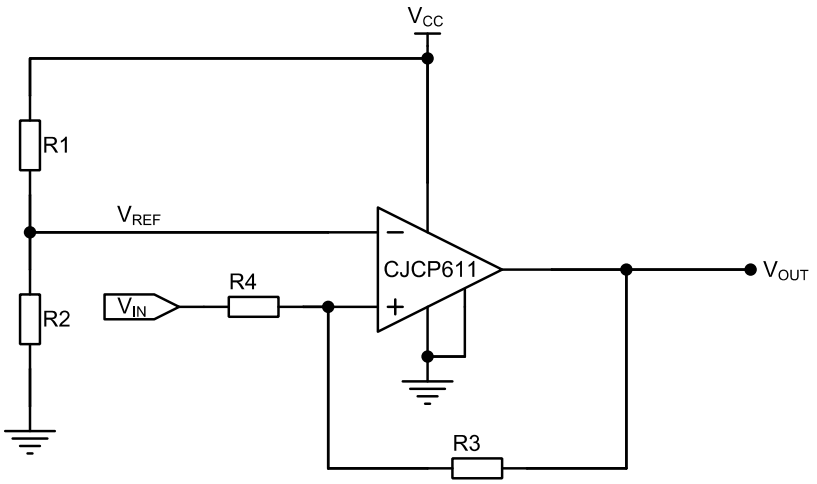


Figure 17: NON-INVERTING CONFIGURATION with Hysteresis

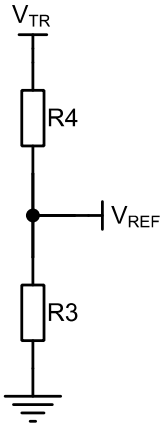


Figure 18: Equivalent circuit of Vin from low to high

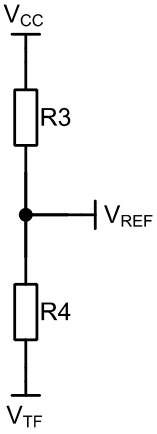


Figure 19: Equivalent circuit of Vin from high to low

8 Application and Implementation

8.1 Typical Application Circuits (continue)

IR Reciever AFE and Wake-Up Circuit

Infrared (IR) communication is inherently immune to RF interference as long as there is a line-of-sight path between the transmitter and the receiver. It is also one of the lowest cost communication schemes. This makes it a good choice for implementing wireless communications in applications such as utility metering. A common system topology to extend battery life is to use a power efficient IR receiver analog front end (AFE) that is always on and wakes up the host only when there is valid IR signal detected as shown in Figure 20.

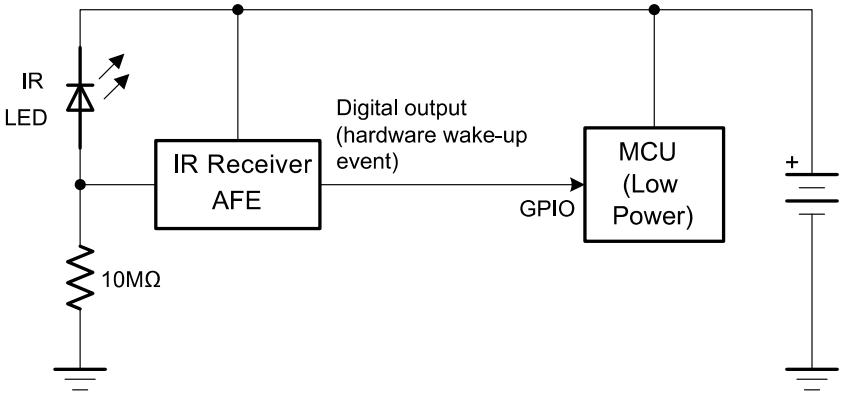


Figure 20: Coin Cell Battery Powered IR Receiver

Power efficient comparators such as the CJCP61x can be used in the IR receiver AFE to increase battery life. The CJCP61x device is responsible for two major tasks:

1. IR signal conditioning
2. Host system wake-up

CJCP61x device is constantly powered to always be ready to receive IR signals and wake up the host microcontroller (MCU) when data is received. The short working distance (approximately 5cm) is suitable for a virtual-contact operation where the IR transmitter and receiver are closely placed with an optional mechanical alignment guide.

Figure 20 shows the IR receiver system block diagram. The host MCU is normally in the shutdown mode (during which the quiescent current is less than 1μA) except when data is being transferred.

Figure 21 shows the detailed circuit design. The circuit established a threshold through R2 and C1 which automatically adapts to the ambient light level. To further reduce BOM cost, this example uses an IR LED as the IR receiver. The IR LED is reverse-biased to function as a photodiode (but at a reduced sensitivity).

The load resistor R1 converts the IR light induced current into a voltage fed into the inverting input of the comparator. R2 and C1 establish a reference voltage V_{REF} which tracks the mean amplitude of the IR signal. The non-inverting input is connected to V_{REF} through R3. And finally R3 and R4 are used to introduce additional hysteresis to keep the output of spurious toggles.

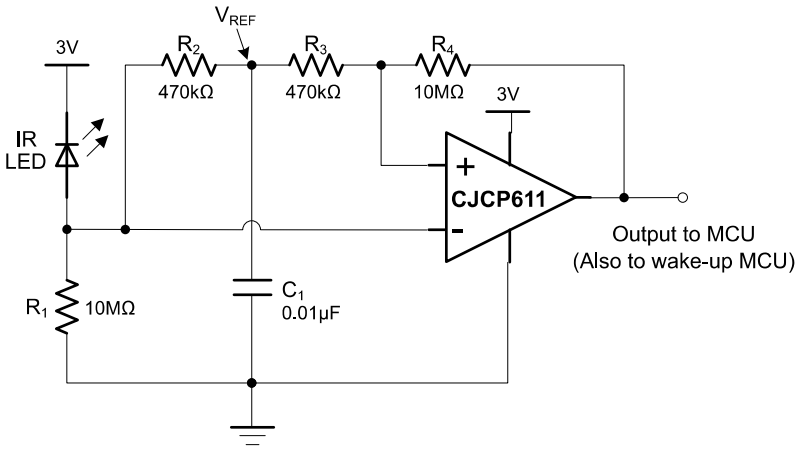


Figure 21: IR Receiver AFE using CJCP611

8 Application and Implementation

8.1 Typical Application Circuits (continue)

Window Comparator

Window Comparators are commonly used to detected undervoltage (UV) and overvoltage (OV) conditions. Figure 22 shows a simple window comparator circuit.

For this design, follow these design requirements:

Alert (logic low output) when an input signal is less than 1.1V

Alert (logic low output) when an input signal is greater than 2.2V

Alert signal is active low

Operate from a 3.3V power supply

Configure the circuit as shown in Figure 22. Connect V_{S+} to a 3.3V power supply and V_{S-} to ground. Make R1, R2 and R3 each 10MΩ resistors. These three resistors are used to create the positive and negative thresholds for the window comparator (VTH+ and VTH-). With each resistor being equal, VTH+ is 2.2V and VTH- is 1.1V. Large resistor values such as 10MΩ are used to minimize power consumption. The sensor output voltage is applied to the inverting and non-inverting inputs of the 2-channel CJCP612's. The respective comparator outputs will be low when the sensor is less than 1.1V or greater than 2.2V. V_{OUT} will be high when the sensor is in the range of 1.1V to 2.2V. See the application curve in Figure 23.

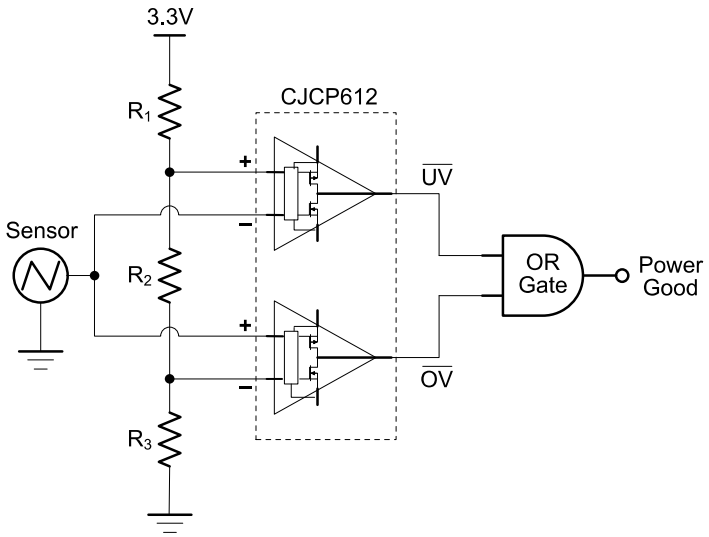


Figure 22: Window Comparator

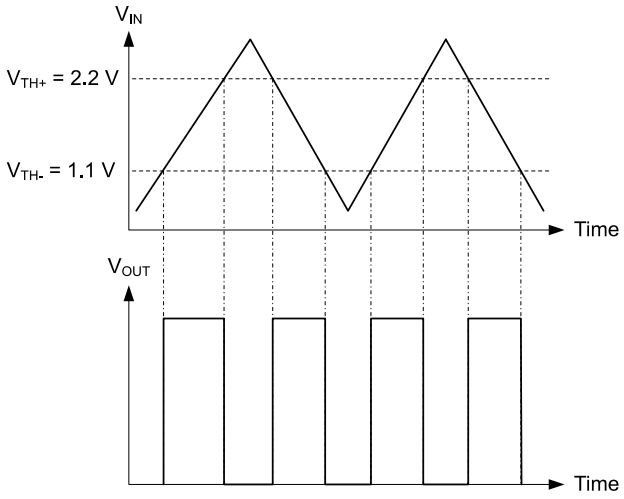


Figure 23: Window Comparator Result

9 Notes and Revision History

9.1 Associated Product Family and Others

To view other products of the same type or IC products of other types, click the official website of SZCJ -- ***http://www.szcjsemi.com*** for more details.

9.2 Notes

Electrostatic Discharge Caution



This IC may be damaged by ESD. Relevant personnel shall comply with correct installation and use specifications to avoid ESD damage to the IC. If appropriate measures are not taken to prevent ESD damage, the hazards caused by ESD include but are not limited to degradation of integrated circuit performance or complete damage of integrated circuit. For some precision integrated circuits, a very small parameter change may cause the whole device to be inconsistent with its published specifications.

9.3 Revision History

December 2025: released CJCP61x Rev - 1.0.

10 Orderable, Mechanical, and Packaging Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

Orderable Information

MODEL	DEVICE	PACKAGE	OP TEMP	ECO PLAN	MSL	PACKING OPTION	SORT
CJCP611	CJCP611-M6N	SOT-23-6L	-40 ~ 125°C	RoHS & Green	Level 3 168 HR	Tape and Reel 3000 Units / Reel	Active
CJCP612	CJCP612-M8N	SOT-23-8L	-40 ~ 125°C	RoHS & Green	Level 3 168 HR	Tape and Reel 3000 Units / Reel	Active
CJCP612	CJCP612-PAN	SOP8	-40 ~ 125°C	RoHS & Green	Level 3 168 HR	Tape and Reel 4000 Units / Reel	Active
CJCP612	CJCP612-PDN	MSOP8	-40 ~ 125°C	RoHS & Green	Level 3 168 HR	Tape and Reel 3000 Units / Reel	Active
CJCP613	CJCP613-M5N	SOT-23-5L	-40 ~ 125°C	RoHS & Green	Level 3 168 HR	Tape and Reel 3000 Units / Reel	Active
CJCP613	CJCP613-R5N	SOT-353	-40 ~ 125°C	RoHS & Green	Level 3 168 HR	Tape and Reel 3000 Units / Reel	Active
Others							Customized

Note:

ECO PLAN: For the RoHS and Green certification standards of this product, please refer to the official report provided by SZCJ

MSL: Moisture Sensitivity Level. Determined according to JEDEC industry standard classification.

SORT: Specifically defined as follows:

Active: Recommended for new products;

Customized: Products manufactured to meet the specific needs of customers;

Preview: The device has been released and has not been fully mass produced. The sample may or may not be available;

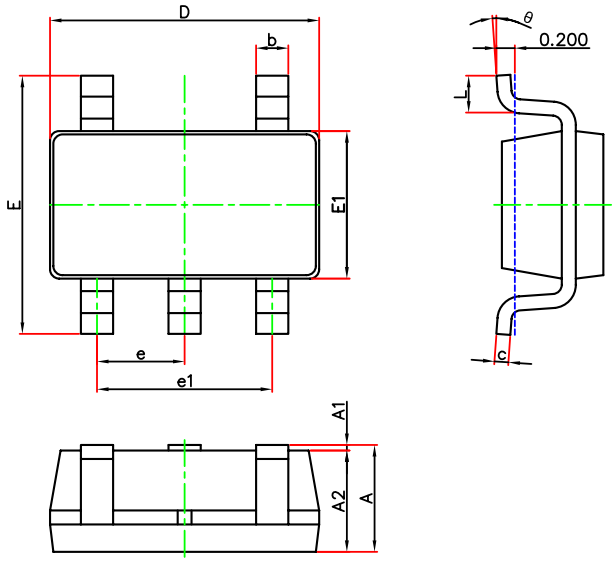
NoRD: It is not recommended to use the device for new design. The device is only produced for the needs of existing customers;

Obsolete: The device has been discontinued.

Mechanical Information

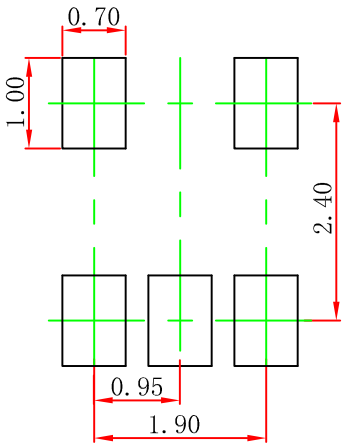
SOT-23-5L Mechanical Information

SOT-23-5L Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.000	1.200	0.039	0.047
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	2.600	3.000	0.102	0.118
E1	1.500	1.700	0.059	0.067
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

SOT-23-5L Suggested Pad Layout

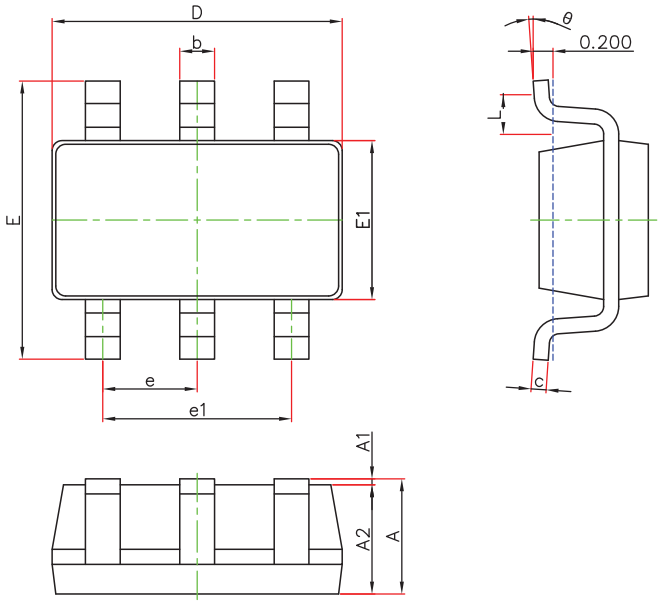


Note:
1. Controlling dimension: in millimeters.
2. General tolerance: ±0.05mm.
3. The pad layout is for reference purpose only.

Mechanical Information

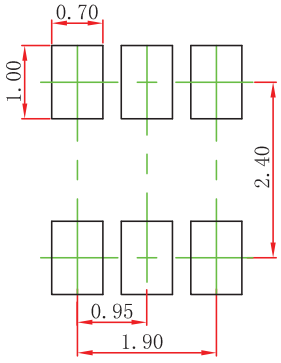
SOT-23-6L Mechanical Information

SOT-23-6L Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	2.650	2.950	0.104	0.116
E1	1.500	1.700	0.059	0.067
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

SOT-23-6L Suggested Pad Layout

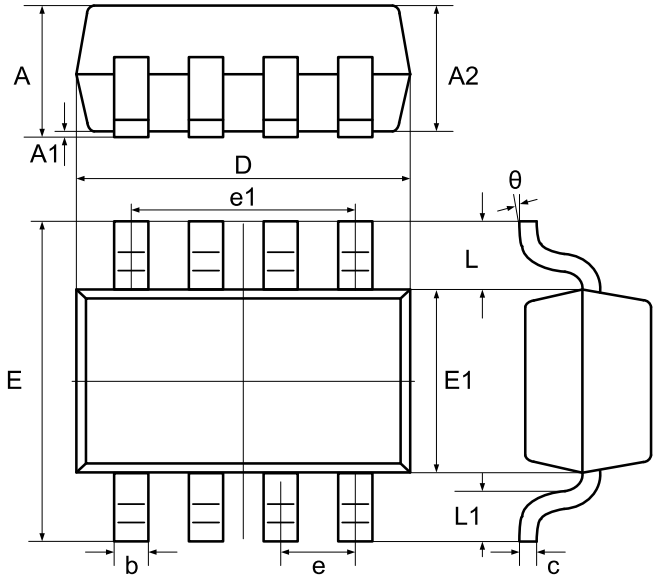


Note:
1. Controlling dimension: in millimeters.
2. General tolerance: ±0.05mm.
3. The pad layout is for reference purpose only.

Mechanical Information

SOT-23-8L Mechanical Information

SOT-23-8L Outline Dimensions

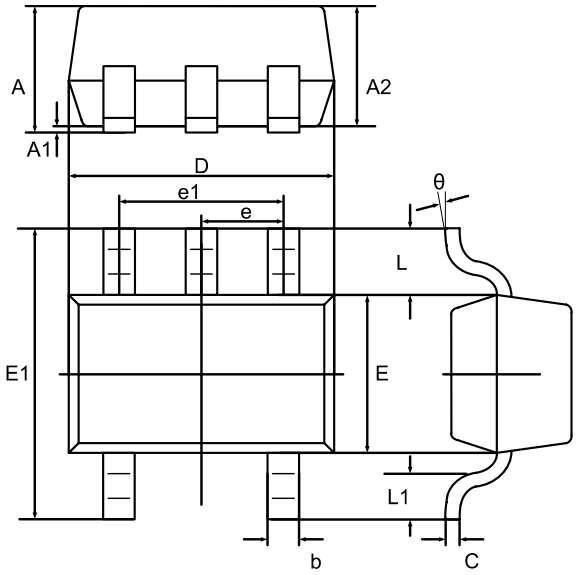


Symbol	Dimensions In Millimeters	
	Min.	Max.
A	0.950	1.450
A1	0.050	0.150
A2	0.900	1.300
b	0.220	0380
c	0.080	0.220
D	2.800	3.000
E	2.600	3.000
E1	1.500	1.700
e	0.650BSC	
e1	1.950BSC	
L	0.600BSC	
L1	0.300	0.600
θ	0°	8°

Mechanical Information

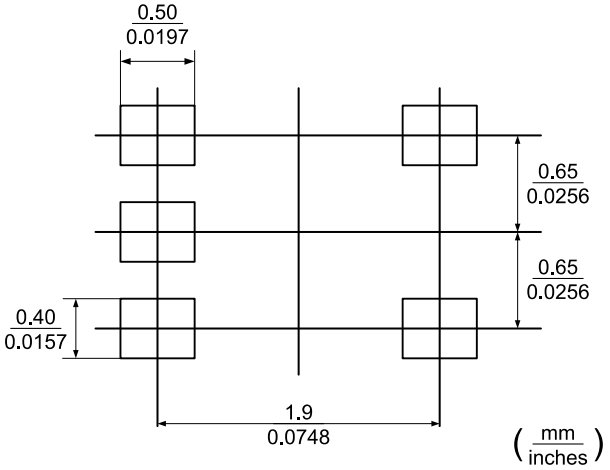
SOT-353 Mechanical Information

SOT-353 Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.90	1.10	0.035	0.043
A1	0.00	0.10	0.000	0.004
A2	0.90	1.00	0.035	0.039
b	0.15	0.35	0.006	0.014
C	0.08	0.15	0.003	0.006
D	2.00	2.20	0.079	0.087
E	1.15	1.35	0.045	0.053
E1	2.15	2.45	0.085	0.096
e	0.65 typ.		0.026 typ.	
e1	1.20	1.40	0.047	0.055
L	0.525 ref.		0.026 ref.	
	0.26	0.46	0.010	0.018
θ	0°	8°	0°	8°

SOT-353 Suggested Pad Layout

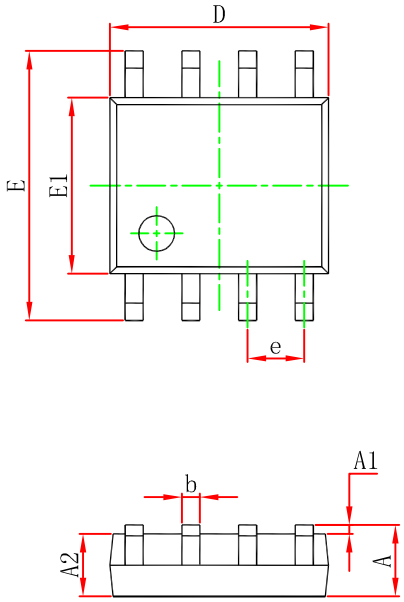


Note:
1. Controlling dimension: in millimeters.
2. General tolerance: ±0.05mm.
3. The pad layout is for reference purpose only.

Mechanical Information

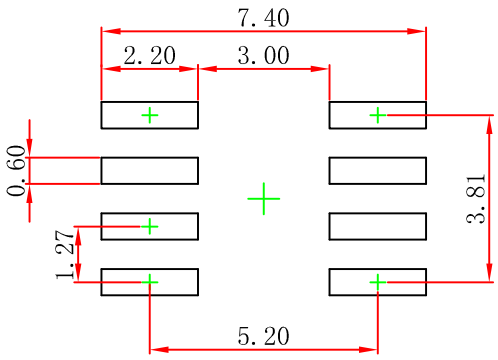
SOP8 Mechanical Information

SOP8 Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.370	1.670	0.054	0.066
A1	0.070	0.250	0.003	0.010
A2	1.350	1.550	0.053	0.061
b	0.300	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
e	1.270(BSC)		0.050(BSC)	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

SOP8 Suggested Pad Layout

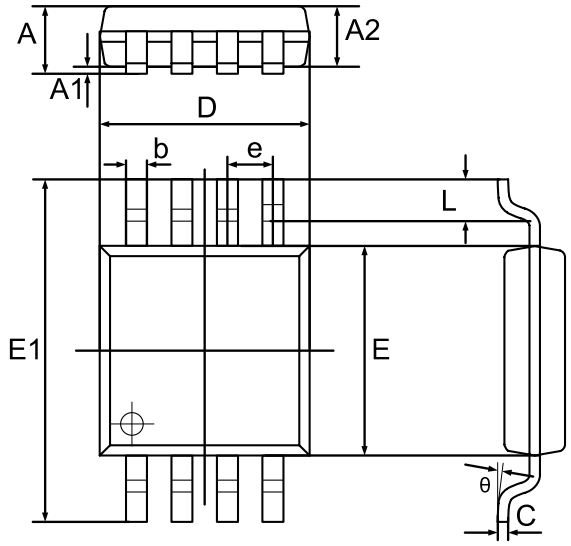


Note:
1. Controlling dimension: in millimeters.
2. General tolerance: ±0.05mm.
3. The pad layout is for reference purpose only.

Mechanical Information

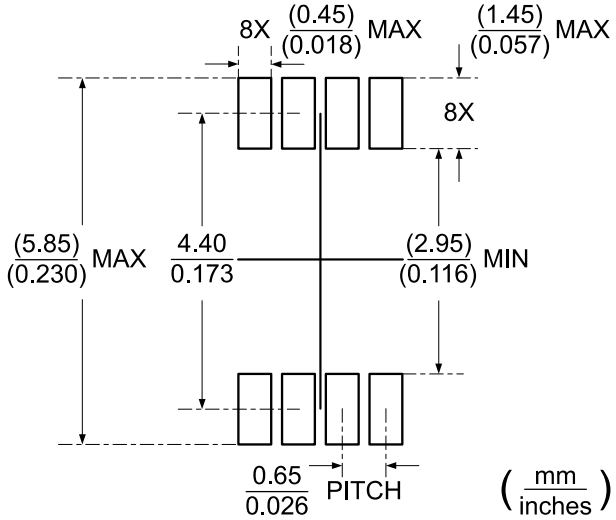
MSOP8 Mechanical Information

MSOP8 Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.800	1.100	0.031	0.043
A1	0.050	0.150	0.002	0.006
A2	0.750	0.950	0.030	0.037
b	0.290	0.380	0.011	0.015
C	0.150	0.200	0.006	0.008
D	2.900	3.100	0.114	0.122
E	2.900	3.100	0.114	0.122
E1	4.700	5.100	0.185	0.201
e	0.650 TYP.		0.026 TYP.	
L	0.400	0.700	0.016	0.028
θ	0°	8°	0°	8°

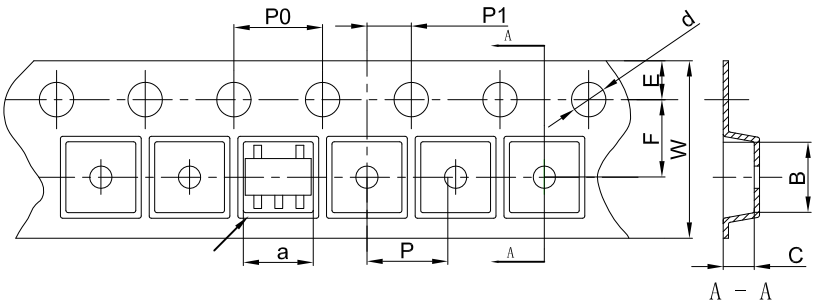
MSOP8 Suggested Pad Layout



Packaging Information

SOT-23-5L Tape and Reel Information

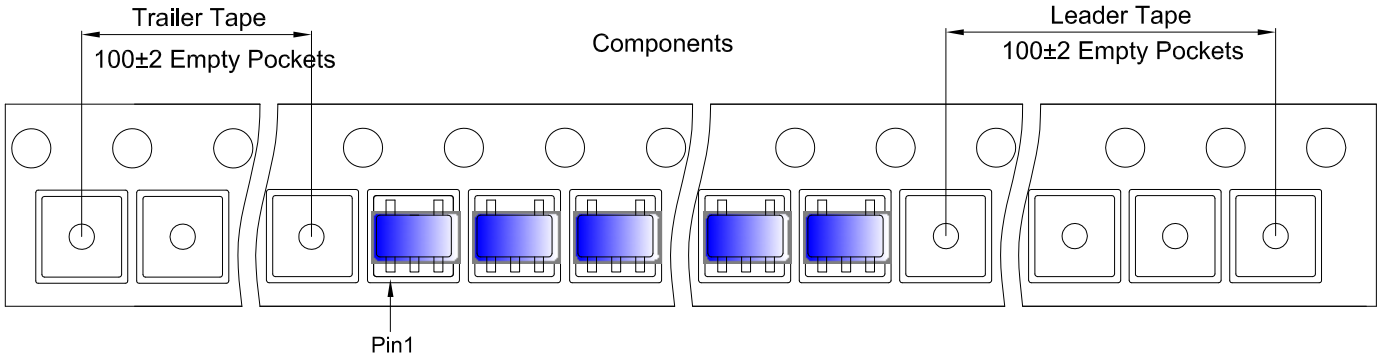
SOT-23-5L Embossed Carrier Tape



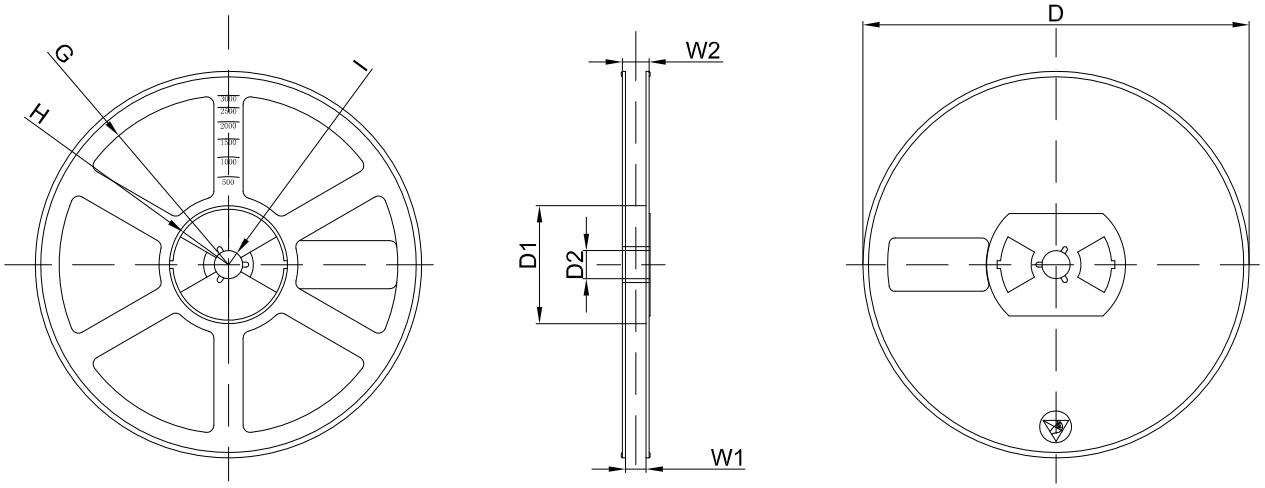
Packaging Description:
SOT-23-5L parts are shipped in tape. The carrier tape is made from a dissipative (carbon filled) polycarbonate resin. The cover tape is a multilayer film (Heat Activated Adhesive in nature) primarily composed of polyester film, adhesive layer, sealant, and anti-static sprayed agent. These reeled parts in standard option are shipped with 3,000 units per 7″ or 18.0cm diameter reel. These reels are clear in color and is made of polystyrene plastic (anti-static coated).

Dimensions are in millimeter										
Pkg type	a	B	C	d	E	F	P0	P	P1	W
SOT-23-5L	3.17	3.23	1.37	Φ1.55	1.75	3.50	4.00	4.00	2.00	8.00

SOT-23-5L Tape Leader and Trailer



SOT-23-5L Reel



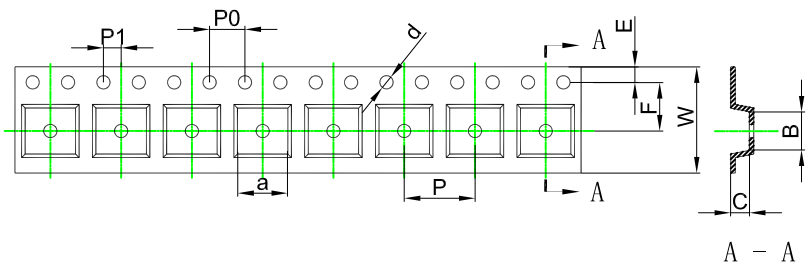
Dimensions are in millimeter								
Reel Option	D	D1	D2	G	H	I	W1	W2
7″Dia	Φ180.00	60.00	13.00	R78.00	R25.60	R6.50	9.50	13.10

REEL	Reel Size	Box	Box size (mm)	Carton	Carton size (mm)	G.W.(kg)
3,000 pcs	7 inch	30,000 pcs	203×203×195	120,000 pcs	430×438×220	

Packaging Information

SOP8 Tape and Reel Information

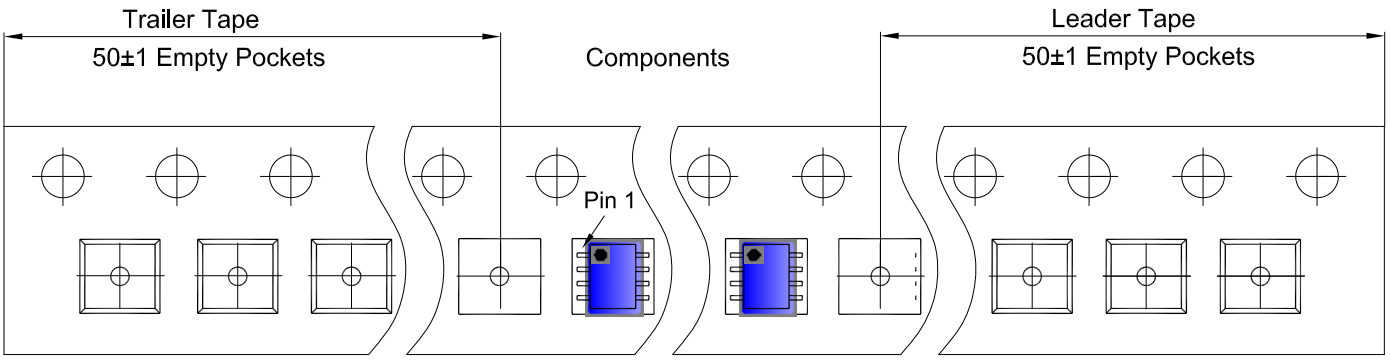
SOP8 Embossed Carrier Tape



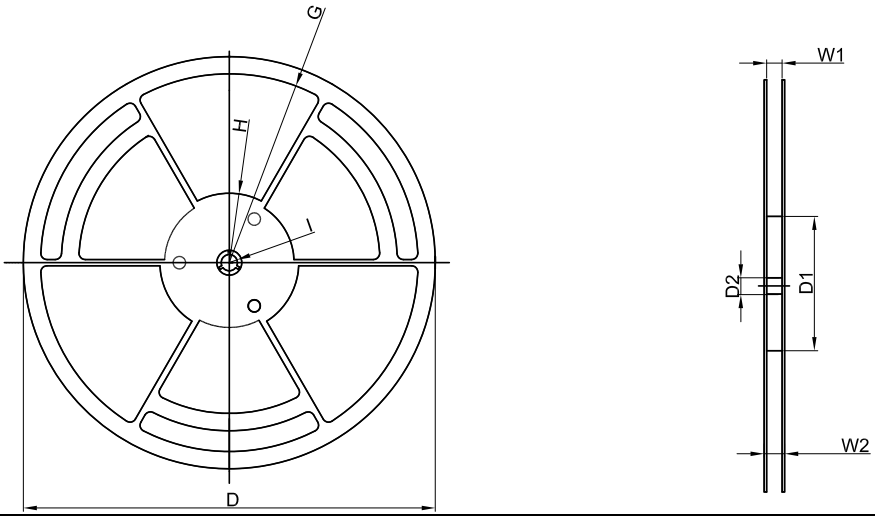
Packaging Description:
SOP8 parts are shipped in tape. The carrier tape is made from a dissipative (carbon filled) polycarbonate resin. The cover tape is a multilayer film (Heat Activated Adhesive in nature) primarily composed of polyester film, adhesive layer, sealant, and anti-static sprayed agent. These reeled parts in standard option are shipped with 2,500 units per 13″ or 33cm diameter reel. These reels are clear in color and is made of polystyrene plastic (anti-static coated).

Dimensions are in millimeter										
Pkg type	a	B	C	d	E	F	P0	P	P1	W
SOP8	6.40	5.40	2.10	Φ1.50	1.75	5.50	4.00	8.00	2.00	12.00

SOP8 Tape Leader and Trailer



SOP8 Reel



Dimensions are in millimeter								
Reel Option	D	D1	D2	G	H	I	W1	W2
13″Dia	Φ330.00	100.00	13.00	R151.00	R56.00	R6.50	12.40	17.60

REEL	Reel Size	Box	Box size (mm)	Carton	Carton size (mm)	G.W.(kg)
4,000 pcs	13 inch	8,000 pcs	360×360×65	64,000 pcs	565×380×390	

DISCLAIMER

IMPORTANT NOTICE, PLEASE READ CAREFULLY

The information in this data sheet is intended to describe the operation and characteristics of our products. SZCJ has the right to make any modification, enhancement, improvement, correction or other changes to any content in this data sheet, including but not limited to specification parameters, circuit design and application information, without prior notice.

Any person who purchases or uses SZCJ products for design shall: 1. Select products suitable for circuit application and design; 2. Design, verify and test the rationality of circuit design; 3. Procedures to ensure that the design complies with relevant laws and regulations and the requirements of such laws and regulations. SZCJ makes no warranty or representation as to the accuracy or completeness of the information contained in this data sheet and assumes no responsibility for the application or use of any of the products described in this data sheet.

Without the written consent of SZCJ this product shall not be used in occasions requiring high quality or high reliability, including but not limited to the following occasions: medical equipment, military facilities and aerospace. SZCJ shall not be responsible for casualties or property losses caused by abnormal use or application of this product.

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