12V Single Channel Full Bridge Motor Driver

CJDR8837E Driver

1 Introduction

CJDR8837E is a 12V, single channel, full bridge motor drive integrated circuit. It supports 12V power input supply voltage and can provide up to 1.9A output current. Its power consumption current is very low in sleep mode. In addition, device integrates functions such as thermal shutdown, under-voltage protection, output short-circuit protection and over-current protection.

CJDR8837E has a PWM (IN1/IN2) input interface which is compatible with industry standard devices. Therefore, it's very suitable for providing integrated motor drive solutions for cameras, consumer products, toys and other low-voltage or battery powered motion control applications.

2 Available Packages

PART NUMBER	PACKAGE
CJDR8837E	SOP8
	DFNWB2x2-8L

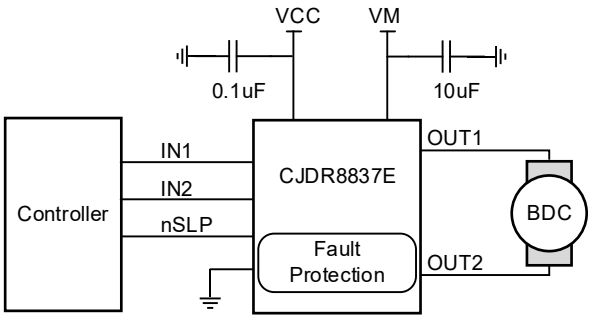
Note: For all available packages, please refer to the part Orderable Information.

3 Features

- N-channel H-bridge motor driver
- 1.8V to 12V Operating Voltage
- Typical RDSON (HS+LS)
  - SOP8 310mΩ
  - DFNWB2x2-8L 290 mΩ
- 1.9A Peak Current Drive
- Standard PWM (IN1/IN2) Interface
- Supports 3.3V, and 5V logic inputs
- Low Consumption Current in Sleep
- Protection features:
  - Undervoltage lockout (UVLO)
  - Overcurrent protection (OCP)
  - Thermal shutdown (TSD)

4 Applications

- Brushed DC motor, solenoid, & relay driving
- Water, gas, & electricity meters
- IP network camera IR cut filter
- Video doorbell
- Electronic smart lock
- Electronic and robotic toys
- Blood pressure monitors
- Electric toothbrush



Simplified schematic

5 Orderable Information

DEVICE	PACKAGE	OP TEMP	ECO PLAN	MSL	PACKING OPTION	SORT
CJDR8837E-AAN	SOP8	-40~125°C	RoHS & Green	Level 3 168 HR	Tape and Reel 4000 Units / Reel	Active
CJDR8837E-DCN	DFNWB2x2-8L	-40~125°C	RoHS & Green	Level 3 168 HR	Tape and Reel 3000 Units / Reel	Active

Note:

ECO PLAN: For the RoHS and Green certification standards of this product, please refer to the official report provided by SZCJ.

MSL: Moisture Sensitivity Level. Determined according to JEDEC industry standard classification.

SORT: Specifically defined as follows:
Active: Recommended for new products;
Customized: Products manufactured to meet the specific needs of customers;
Preview: The device has been released and has not been fully mass produced. The sample may or may not be available;
NoRD: It is not recommended to use the device for new design. The device is only produced for the needs of existing customers;
Obsolete: The device has been discontinued.

6 Pin Configuration and Marking Information

6.1 Pin Configuration

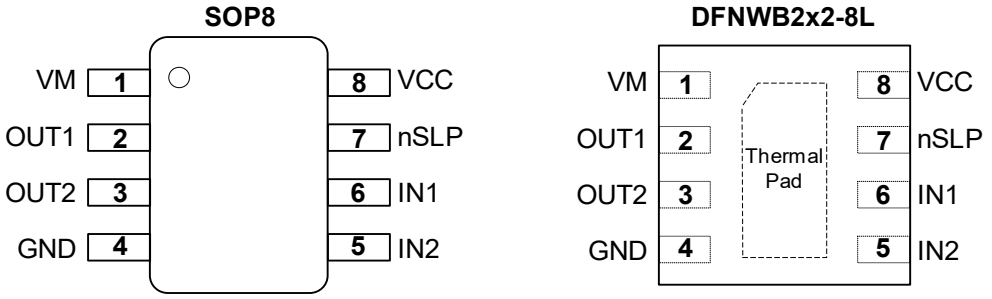


Figure 6-1 Pin configuration

6.2 Pin Function

PIN		I/O(1)	DESCRIPTION
No.	NAME		
1	VM	P	Motor power supply. Connect a 0.1μF bypass capacitor to ground, as well as sufficient bulk capacitance (≥10μF recommended).
2	OUT1	O	H-bridge output. Connect directly to the motor or other inductive load.
3	OUT2	O	H-bridge output. Connect directly to the motor or other inductive load.
4	GND	G	Device ground. Connect to system ground.
5	IN2	I	Logic inputs. Controls the H-bridge output. Has internal pulldowns.
6	IN1	I	Logic inputs. Controls the H-bridge output. Has internal pulldowns.
7	nSLP	I	Sleep mode input. Set this pin to logic high to enable the device. Set this pin to logic low to go to low-power sleep mode. Internal pulldown resistor.
8	VCC	P	Logic power supply. Bypass this pin to the GND pin with a 0.1μF ceramic capacitor rated for V_{CC}.

(1) I-Input, O-Output, P-Power, G-Ground

6.3 Marking Information



8837E: Device code
YYYY: Date Code.

7 Specifications

7.1 Absolute Maximum Ratings

Over operating ambient temperature range (unless otherwise noted)(1)(2)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_M	Motor power supply voltage	-0.3	14	V
V_{CC}	Logic power supply voltage	-0.3	6	V
IN1, IN2, nSLP	Logic input voltage	-0.3	6	V
OUT1, OUT2	Output pin voltage	$-V_D$	V_M+V_D	V
I_{OUT}	Output current	Internal limited		A
T_J	Operating junction temperature	-40	150	°C
T_{STG}	Storage temperature	-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to network ground terminal.

7.2 Recommended Operating Conditions

Over operating ambient temperature range (unless otherwise noted) (1)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_M	Motor power supply voltage	1.8	12	V
V_{CC}	Logic power supply voltage	1.8	5.5	V
V_I	Logic input voltage (IN1, IN2, nSLP)	0	5.5	V
I_{PEAK}	Peak output current	0	1.9	A
f_{PWM}	Logic input PWM frequency	0	100	kHz
T_A	Operating ambient temperature	-40	125	°C

(1) Recommended Operating Conditions indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications, see the Electrical Characteristics.

7.3 ESD Ratings

SYMBOL	ESD RATINGS		VALUE	UNIT
$V_{ESD-HBM}$	Electrostatic discharge(1)	Human body model (HBM)	±4000	V
$V_{ESD-CDM}$	Electrostatic discharge(2)	Charged Device Model (CDM)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP155 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.4 Thermal Information

SYMBOL	THERMAL METRIC	SOP8	DFNWB2x2-8L	UNIT
$R_{\Theta JA}$(1)	Junction to ambient thermal resistance	110	79	°C/W
$R_{\Theta JA(EVM)}$(2)	Junction to ambient thermal resistance. (Specific EVM)	77	45	°C/W

(1) The value given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were measured on JESD 51-7, 4-layer JEDEC PCB board.

(2) Based on the thermal resistance information measured on the EVM: 80mm x 80mm, FR-4, TG150, 1.6mm thickness, 2-layer 2-0z Cu copper. This thermal resistance information is for reference only. The actual thermal resistance depends on PCB board, layout, and test environment conditions.

7.5 Electrical Characteristics

T_A=25°C, over recommended operating conditions (unless otherwise noted).

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
Power Supply (VM, VCC)							
V_M	VM operating voltage	-		1.8	-	12	V
I_{VM}	VM active mode current	V_M=5V, V_{CC}=nSLP=3.3V		-	1.3	2.5	mA
I_{VM_OFF}	VM sleep current	V_M=5V, V_{CC}=3.3V, Sleep mode		-	40	100	nA
V_{CC}	VCC operating voltage	-		1.8	-	5.5	V
I_{CC}	VCC active mode current	V_M=5V, V_{CC}=nSLP=3.3V		-	2	10	uA
I_{CC_OFF}	VCC sleep current	V_M=5V, V_{CC}=3.3V, INx=nSLP=0V		-	1	25	nA
t_{WAKE}(1)	Time to wake	Sleep mode to active mode delay		10	25	50	us
Motor Driver Outputs (OUT1, OUT2)							
R_{DSON}	High-side FET on resistance	V_M=5V, V_{CC}=3.3V, I_{OUT}=0.2A	SOP8	-	160	-	mΩ
			DFNWB2x2-8L	-	150	-	mΩ
R_{DSON}	Low-side FET on resistance	V_M=5V, V_{CC}=3.3V, I_{OUT}=0.2A	SOP8	-	150	-	mΩ
			DFNWB2x2-8L	-	140	-	mΩ
I_{OFF}	Off-state leakage current	OUTx Hi-Z, R_L=20Ω		-200	-	200	nA
t_R(1)	Output rise time	OUTx rising from 10% to 90% of V_M		-	50	-	ns
t_F(1)	Output fall time	OUTx falling from 90% to 10% of V_M		-	50	-	ns
t_{PD1}(1)	Propagation delay	INx to OUTx High/Low change		-	150	-	ns
t_{PD2}(1)	Propagation delay, including dead time	INx to OUTx High/Low change		-	300	-	ns
t_{EN}(1)	Enable delay	INx to OUTx High/low change		-	50	-	ns
t_{DIS}(1)	Disable delay	INx to OUTx High-Z change		-	130	-	ns
Logic-Level Inputs (IN1, IN2, nSLP)							
V_{IH}	Input logic high voltage threshold	-		-	0.4V_{CC}	0.6V_{CC}	V
V_{IL}	Input logic low voltage threshold	-		0.25V_{CC}	0.38V_{CC}	-	V
V_{I_HYS}	Input logic hysteresis	-		-	80	-	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{IH}	Input logic high current	IN=3.3V	-	28	50	uA
I_{IL}	Input logic low current	IN=0V	-1	-	1	uA
R_{PD}	Pulldown resistance	IN1, IN2, nSLP To GND	60	120	200	kΩ
Protection Circuits						
V_{UVLO_VCC}	VCC supply undervoltage lockout	Supply rising	-	-	1.8	V
		Supply falling	-	-	1.7	V
V_{UVLO_Hys}	VCC undervoltage hysteresis	-	-	100	-	mV
I_{OCP}	Overcurrent protection trip level	-	1.9	-	-	A
t_{OCP}(1)	Overcurrent deglitch time	-	-	2	-	us
t_{RETRY}(1)	Overcurrent retry time	-	-	1	-	ms
T_{SD}(1)	Thermal shutdown temperature	-	150	-	-	°C
T_{HYS}(1)	Thermal shutdown hysteresis	-	-	40	-	°C

(1) Guaranteed by design, not tested.

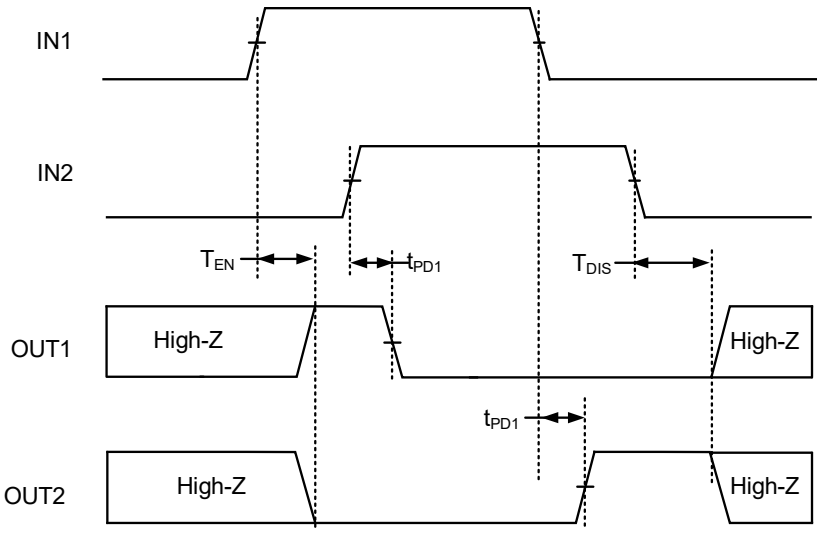


Figure 7-1 PWM timing

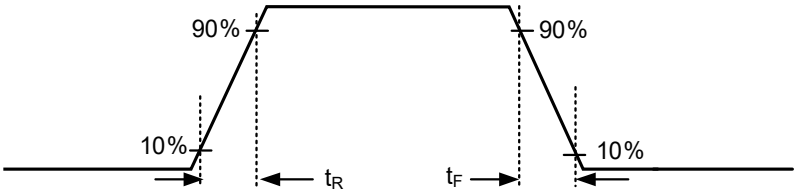


Figure 7-2 Edge timing

8 Detailed Description

8.1 Overview

CJDR8837E is a 12V, single channel, full bridge motor drive integrated circuit. It supports 12V power input supply voltage and can provide up to 1A continuous output current. In sleep mode, its power consumption current is less than 100nA. In addition, it integrates functions such as thermal shutdown, under-voltage protection, output short-circuit protection and over-current protection.

CJDR8837E has a PWM (IN1/IN2) input interface which is compatible with industry standard devices.

8.2 Functional Block Diagram

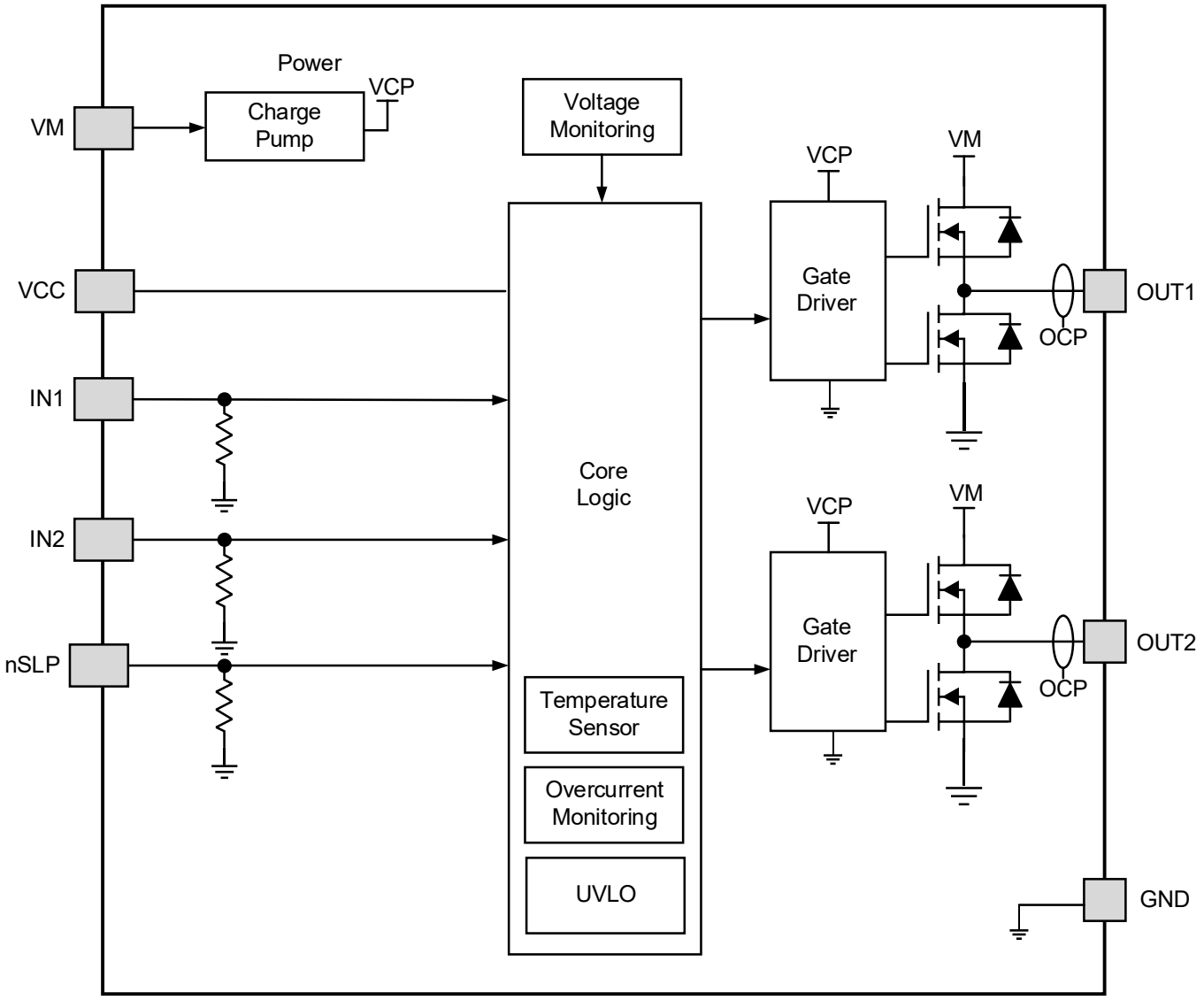


Figure 8-1 Block diagram

8.3 Bridge Control

8.3.1 Control Logic

The CJDR8837E provides interface to achieve different functions and control logic. The inputs can be set to static voltages for 100% duty cycle drive, or they can be pulse-width modulated (PWM) for variable motor speed. Device could control the motor to work in forward, reverse condition. Alternatively, the coast mode for fast current decay or brake mode for slow low side current decay are also available.

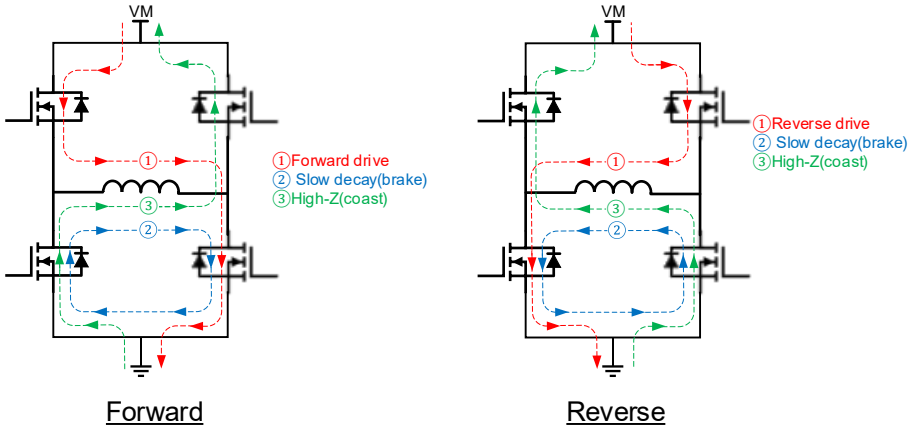


Figure 8-2 H-Bridge current paths

For CJDR8837E, PWM interface, also called IN1/IN2 interface, is available. Both pin have 100k pull down resistor.

Table 8-1 shows the control logic.

Table 8-1 CJDR8837E control logic

nSLP	IN1	IN2	OUT1	OUT2	DESCRIPTION
0	x	x	High-Z	High-Z	Coast (H-bridge disabled to High-Z); Sleep mode entered immediately
1	0	0	High-Z	High-Z	Coast (H-bridge disabled to High-Z)
1	0	1	L	H	Reverse (Current OUT2 → OUT1)
1	1	0	H	L	Forward (Current OUT1 → OUT2)
1	1	1	L	L	Brake (low-side slow decay)

8.3.2 Sleep Mode

A dedicated sleep mode control pin is used for CJDR8837E with 120kohm pull down resistor. If the nSLP pin is brought to a logic-low state, a low-power sleep mode is entered. In this state, all unnecessary internal circuitry is powered down.

8.4 Protection Circuits

The device is fully protected against undervoltage, output overcurrent, and overtemperature events.

8.4.1 Supply Undervoltage Lockout (UVLO)

If at any time the VCC supply voltage falls below the undervoltage-lockout (UVLO) threshold voltage, all MOSFETs in the H-bridge will be disabled. Operation resumes when voltage rises above the UVLO threshold. The charge pump and device logic are disabled in this condition.

8.4.2 Overcurrent Protection (OCP)

All MOSFETs in the H-bridge are disabled if the output current exceeds the OCP threshold, I_{OCP}, for longer than t_{OCP}. These overcurrent conditions are detected independently on both high-side and low-side MOSFETs. Which means that a short to ground, supply, or across the motor winding will all result in an overcurrent shutdown. When OCP triggered, H-bridge are disabled for a duration of t_{RETRY}. After that, the H-bridge is re-enabled according to the state of the INx pins. If the overcurrent fault is still present, the cycle repeats, otherwise normal device operation resumes.

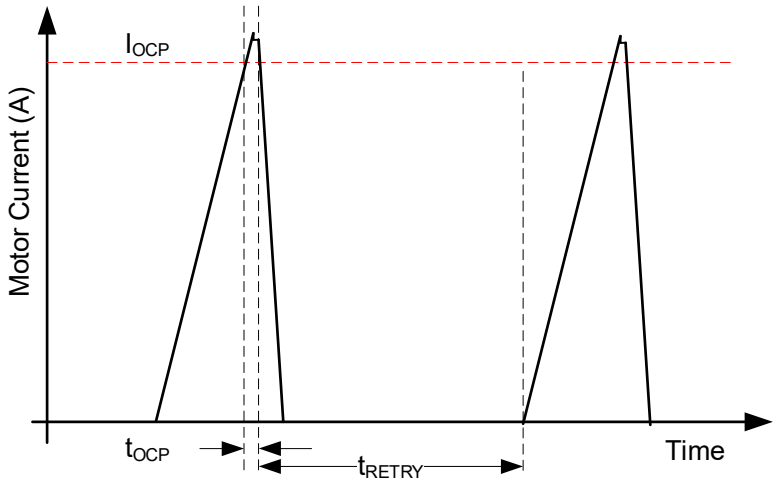


Figure 8-3 OCP timing

8.4.3 Thermal Shutdown (TSD)

If the die temperature exceeds safe limits T_{SD}, all MOSFETs in the H-bridge are disabled. After the die temperature has fallen to a safe level, operation automatically resumes.

8.4.4 Protection Recovery

The device enters a fault mode when a fault is encountered. This protects the device and the output load. The device behavior in the fault mode is described in Section 8.3.3 and depends on the fault condition. The device leaves the fault mode and re-enters the active mode once the recovery condition is met. Table 8-2 summarizes the fault conditions, response, and recovery.

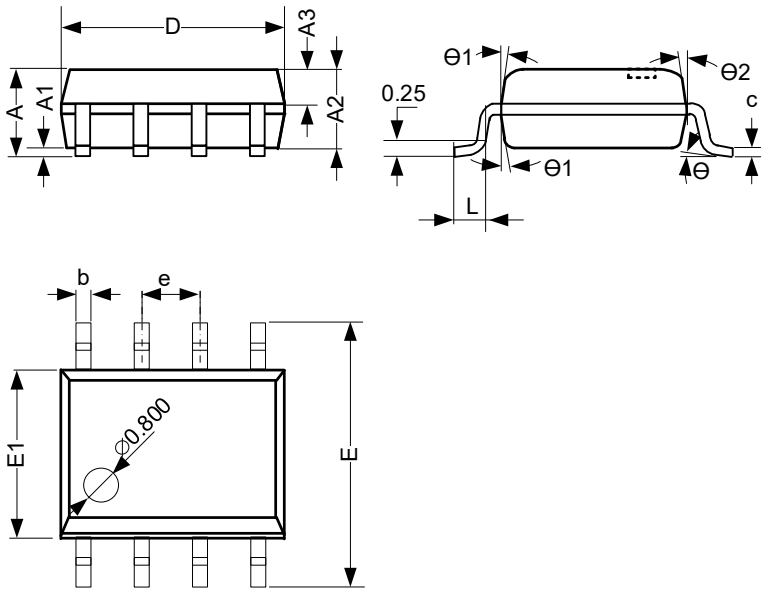
Table 8-2 Fault and recovery

FAULT	CONDITION	H-BRIDGE	RECOVERY
Undervoltage Lockout (UVLO)	$V_{CC}<V_{UVLO_VCC}$, falling	Disabled	$V_{CC}>V_{UVLO_VCC}$, rising
Overcurrent (OCP)	$I_{OUT}>I_{OCP}$	Disabled	t_{RETRY}
Thermal Shutdown (TSD)	$T_J>T_{SD}$	Disabled	$T_J<T_{SD}-T_{HYS}$

9 Mechanical Information

9.1 SOP8 Mechanical Information

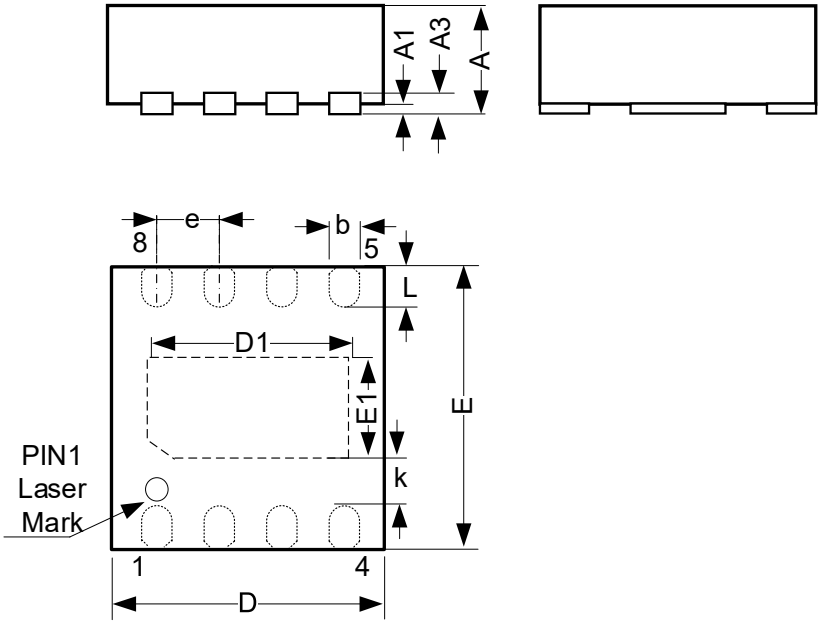
9.1.1 SOP8 Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	1.300	1.500	1.700
A1	0.100	0.150	0.200
A2	1.350	1.420	1.550
A3	0.660	0.670	0.680
b	0.330	0.400	0.510
c	0.170	0.203	0.250
D	4.800	4.900	5.000
E	5.800	6.000	6.200
E1	3.800	3.900	4.000
e	1.270 BSC		
L	0.50	0.65	0.80
L1	1.05 REF		
Θ	0°	3°	8°
Θ1	12° REF		
Θ2	12° REF		
Unit：mm			

9.2 DFNWB2x2-8L Mechanical Information

9.2.1 DFNWB2x2-8L Outline Dimensions



SYMBOL	Dimensions In Millimeters		
	Min.	Typ.	Max.
A	0.700	0.750	0.800
A1	0.000	0.020	0.050
A3	0.203 REF		
b	0.200	0.250	0.300
D	1.900	2.000	2.100
D1	1.500	1.600	1.700
E	1.900	2.000	2.100
E1	0.700	0.800	0.900
e	0.500 BSC		
L	0.250	0.300	0.350
k	0.300 REF		
Unit：mm			

10 Notes and Revision History

10.1 Associated Product Family and Others

To view other products of the same type or IC products of other types, click the official website of SZCJ -- ***https:www.szcjsemi.com m*** for more details.

10.2 Notes

Electrostatic Discharge Caution



This IC may be damaged by ESD. Relevant personnel shall comply with correct installation and use specifications to avoid ESD damage to the IC. If appropriate measures are not taken to prevent ESD damage, the hazards caused by ESD include but are not limited to degradation of integrated circuit performance or complete damage of integrated circuit. For some precision integrated circuits, a very small parameter change may cause the whole device to be inconsistent with its published specifications.

10.3 Revision History

May 2026: CJDR8837E rev - 1.3 change SOP8 Tape and Reel information from 3000 Units / Reel to 4000 Units / Reel; Add JEDEC thermal resistance;

DISCLAIMER

IMPORTANT NOTICE, PLEASE READ CAREFULLY

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